Bidirectional SHIFT REGISTERs

Digital Logic Design (CC131)

BSCS 2nd Semester Spring-2026

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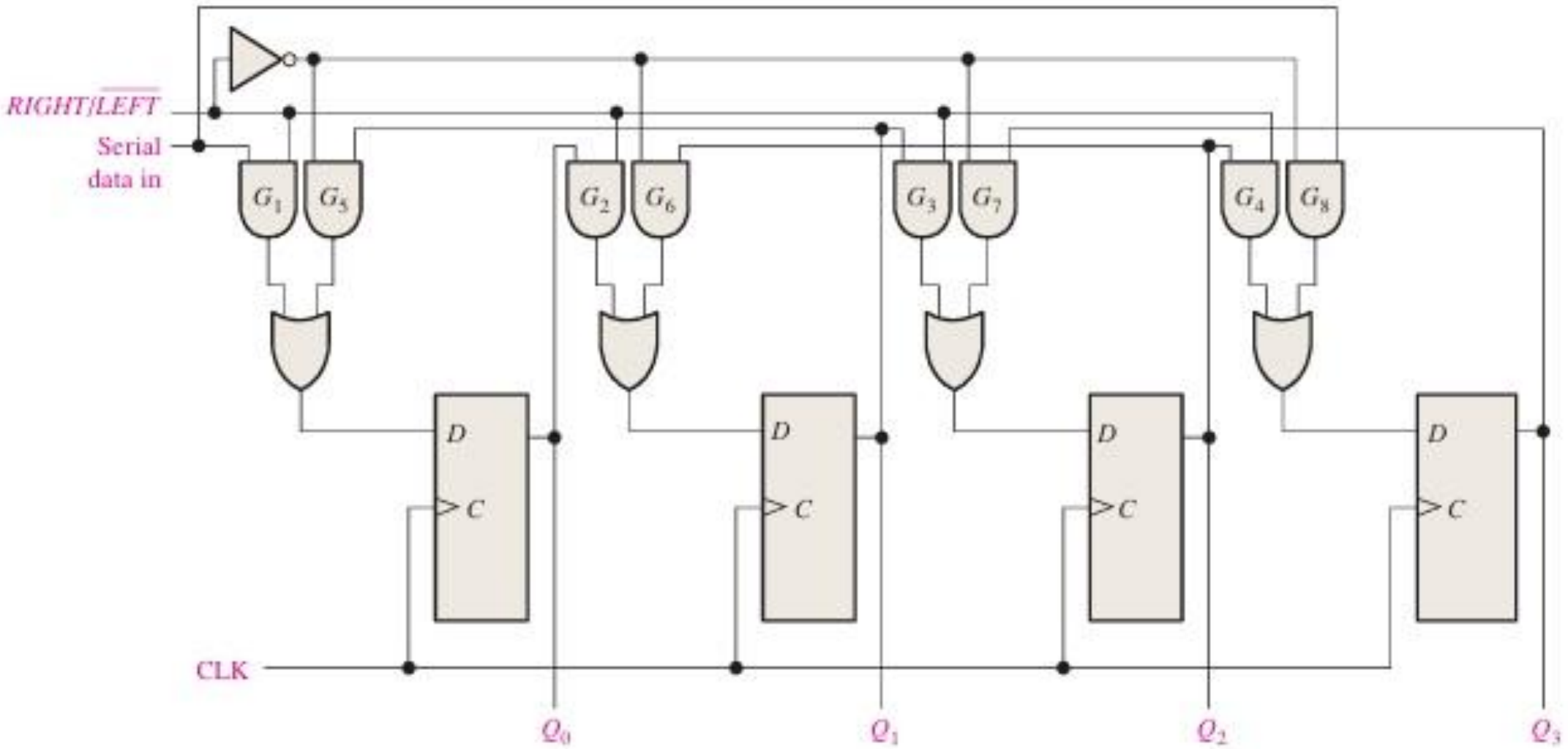
Bidirectional Shift Register

- A Bidirectional Shift Register can shift the data bits either right or left.
- The direction of the movement is controlled by a control line.
- When this control line is HIGH, bits move towards RIGHT one-step per clock pulse.
- When this control line is LOW bits move towards LEFT one-step per clock pulse.

4-Bit Bidirectional Shift Register

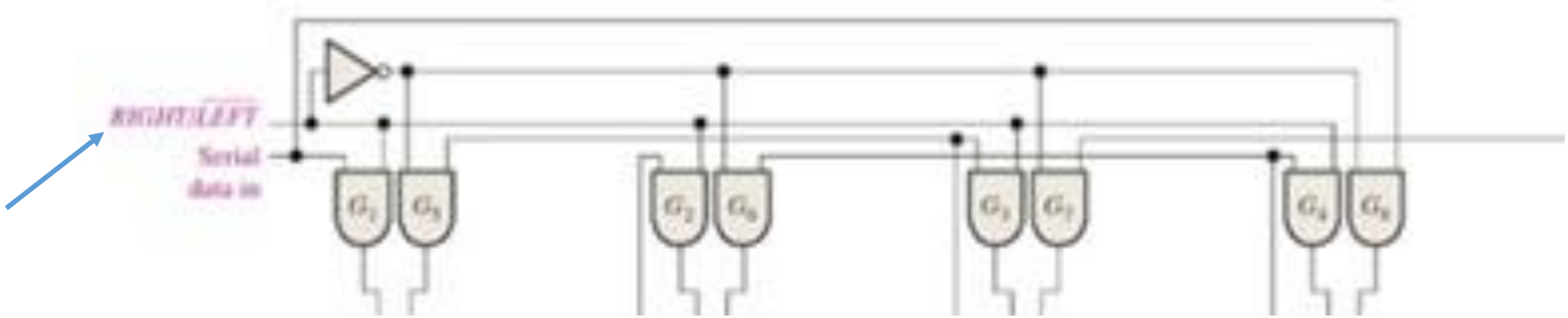


Operation of a
4-Bit Bidirectional Shift Register

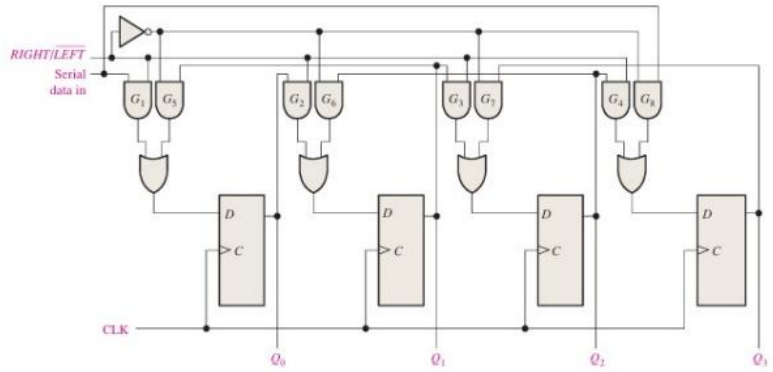
1. Understanding The Control Line (RIGHT / $\overline{\text{LEFT}}$)

The mode of operation is entirely decided by the single **RIGHT / $\overline{\text{LEFT}}$** control line, which acts like a steering switch.

- The line connects **directly** to one set of AND gates (G1 to G4).
- The line passes through an **inverter (NOT gate)** before connecting to the other set of AND gates (G5 to G8).
- This ensures that when one set of gates is active (enabled), the other set is completely deactivated (disabled).



2. Shifting RIGHT (Control Line = HIGH)



When the RIGHT/$\overline{\text{LEFT}}$ control input is set to **HIGH (1)**:

- **Gate Activation:** Gates **G1, G2, G3, and G4** turn ON.
  Gates G5 through G8 are forced OFF.

- **Data Path:** Serial data enters through G1 into the first flip-flop (Q_0).
  The output of each flip-flop is passed forward to the next one (e.g. Q_0 passes through G2 into D_1, Q_1 passes through G3 into D_2, and so on).

- **Result:** On the next clock pulse, all data bits take one step to the **right** ($Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$).

3. Shifting LEFT (Control Line = LOW)

When the RIGHT/LEFT control input is set to **LOW (0)**:

- **Gate Activation:** The NOT gate inverts the signal to HIGH, turning ON gates **G5, G6, G7 and G8**.
  Gates G1 through G4 are turned OFF.

- **Data Path:** The data path reverses direction.
  The output of a succeeding flip-flop is fed backward into the preceding one (e.g., Q_3 passes through G7 back into D_2, Q_2 passes through G6 back into D_1, and Q_1 passes through G5 back into D_0).

- **Result:** On the next clock pulse, all data bits take one step to the **left** ($Q_3 \rightarrow Q_2 \rightarrow Q_1 \rightarrow Q_0$).

4. DATA ENTRY

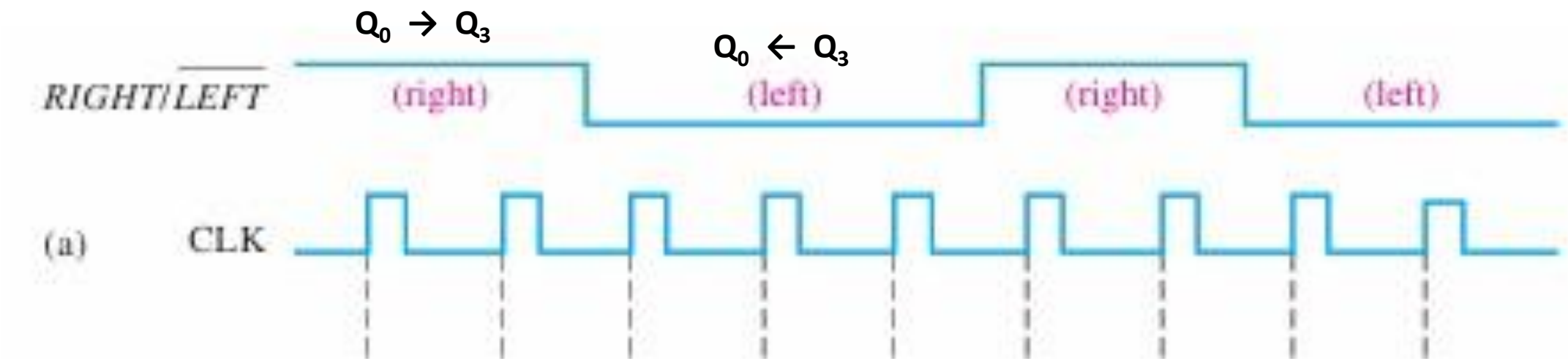
- When the present data bits move towards RIGHT one-step per clock pulse, a vacant position will be created at LSB. This vacant position will be filled with whatever data is present on the Serial Data Input line.

- Similarly, when the current data bits move towards LEFT one-step per clock pulse, a vacant position will be created at MSB. This vacant position will be filled with whatever data is present on the Serial Data Input line.

EXAMPLE

EXAMPLE 8–4

Determine the state of the shift register of Figure 8–17 after each clock pulse for the given *RIGHT*/$\overline{LEFT}$ control input waveform in Figure 8–18(a). Assume that $Q_0 = 1$, $Q_1 = 1$, $Q_2 = 0$, and $Q_3 = 1$ and that the serial data-input line is LOW.



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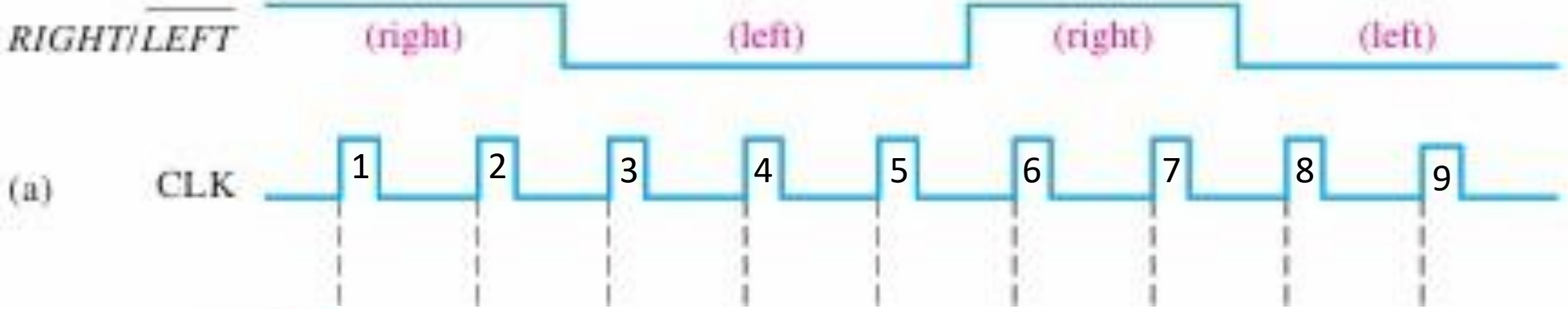
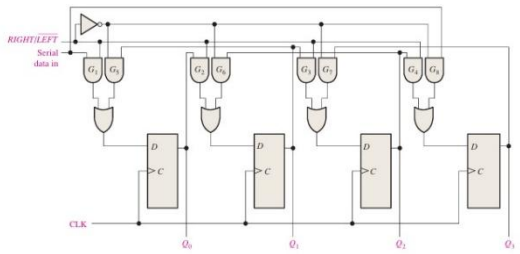
SOLUTION





LSB Q_0 1

Q_1 1

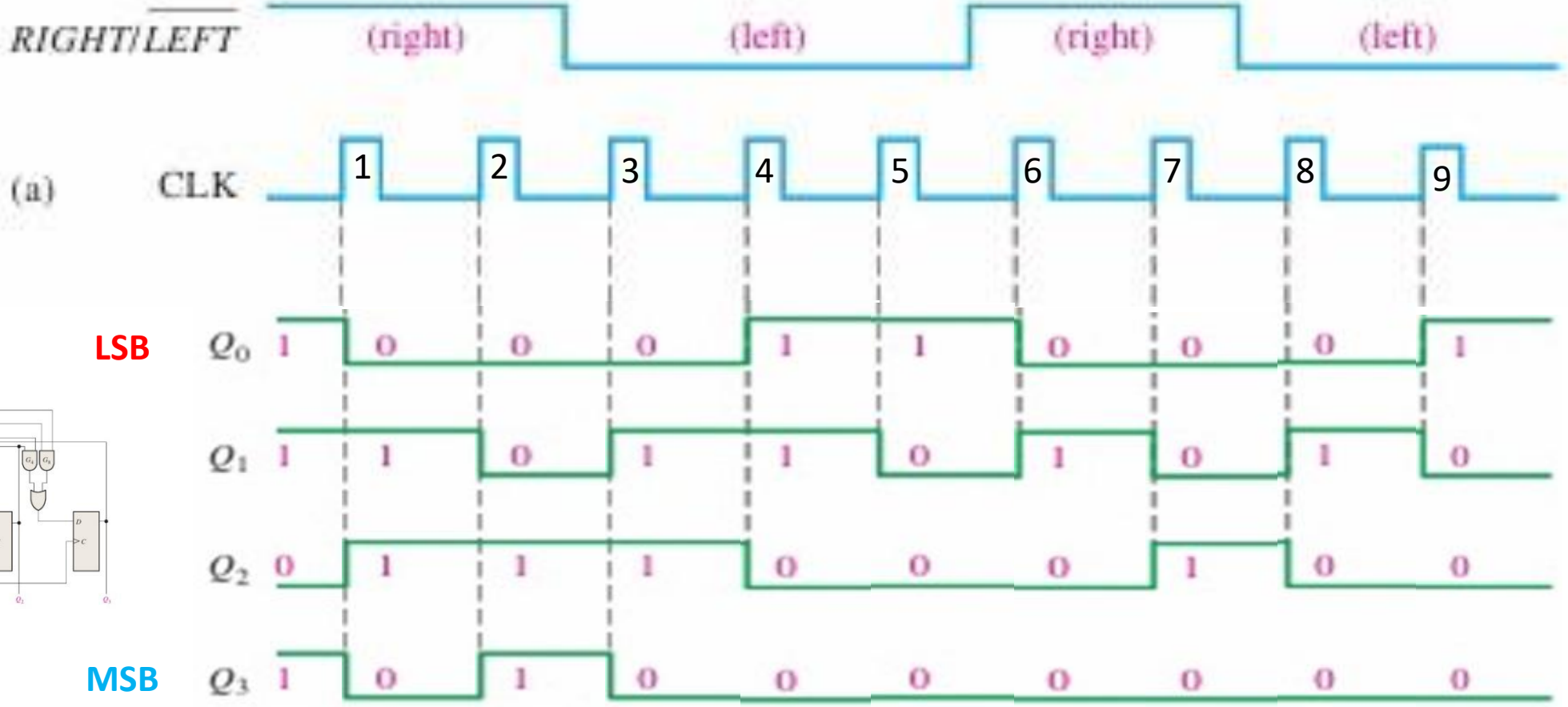
Q_2 0

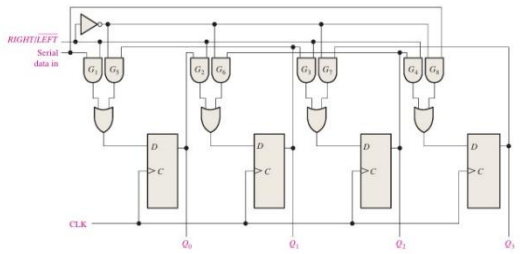
MSB Q_3 1

EXAMPLE 8–4

Determine the state of the shift register of Figure 8–17 after each clock pulse for the given *RIGHT*/$\overline{LEFT}$ control input waveform in Figure 8–18(a). Assume that $Q_0 = 1$, $Q_1 = 1$, $Q_2 = 0$, and $Q_3 = 1$ and that the serial data-input line is LOW.

SOLUTION





SUMMARY

1. A bidirectional shift register can move data either left or right depending on the voltage level of a single RIGHT/LEFT control line.

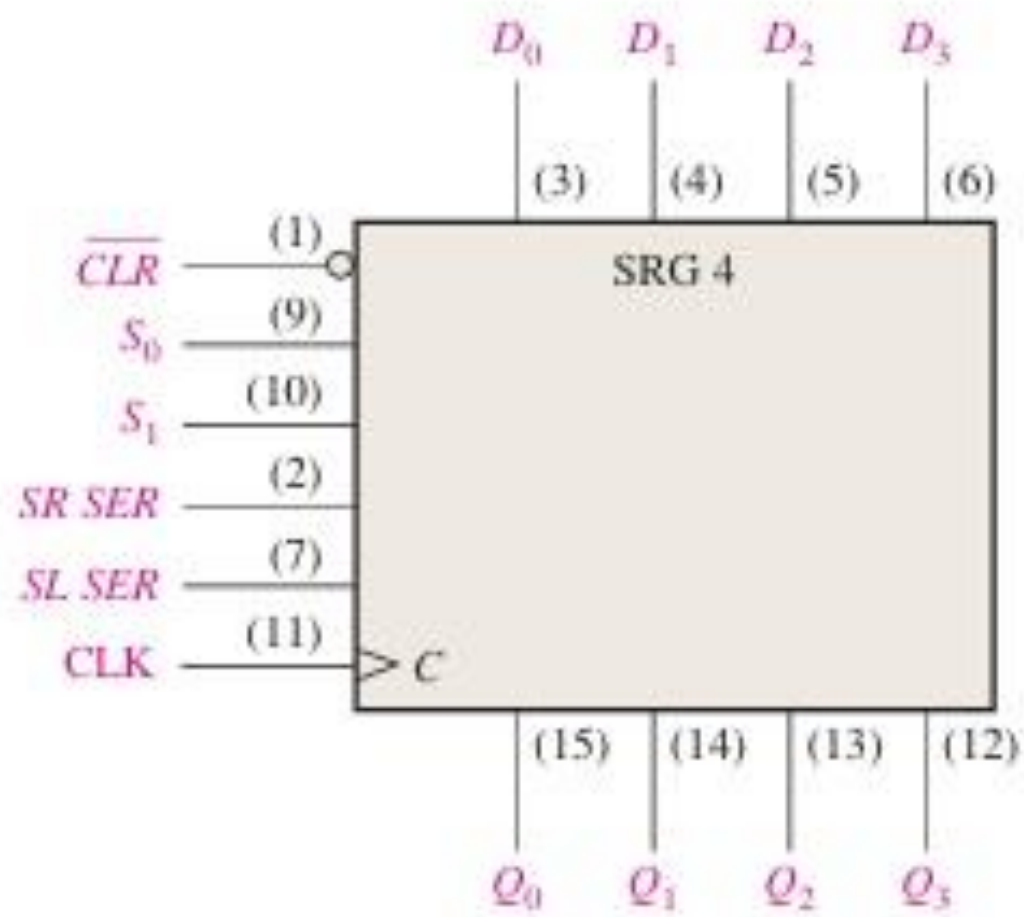
2. When the control line is HIGH, the top set of AND gates (G1 to G4) activates to enable right-shifting logic.

3. During a right shift, external data enters the first flip-flop (Q_0 or LSB), while all existing bits step one position to the right on each clock pulse.

4. When the control line is LOW, an inverter activates the bottom set of AND gates (G5 to G8) to enable left-shifting logic.

5. During a left shift, external data enters the last flip-flop (Q_3 or MSB) via gate G8, while the other bits move backward to the left.

FIGURE 8–19 The 74HC194 4-bit bidirectional universal shift register.



Thank You