

TYPES OF GATED LATCH

Digital Logic Design (CC131)

BSCS 2nd Semester Spring-2026

Lecture: Week8-b

By

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TYPES OF GATED LATCH

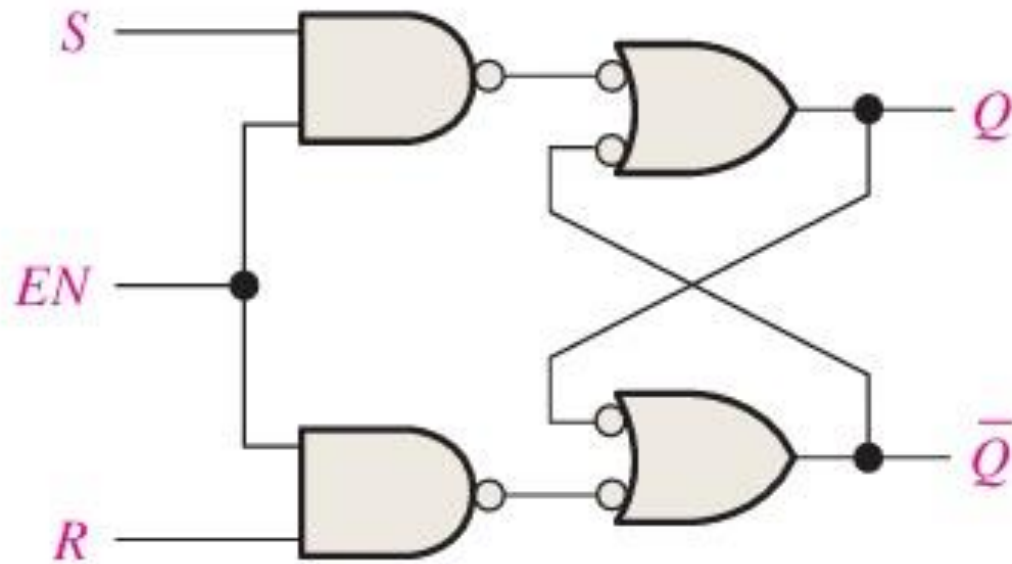
There are two types of gated latches.

1. Gated S-R Latch
2. Gated D Latch

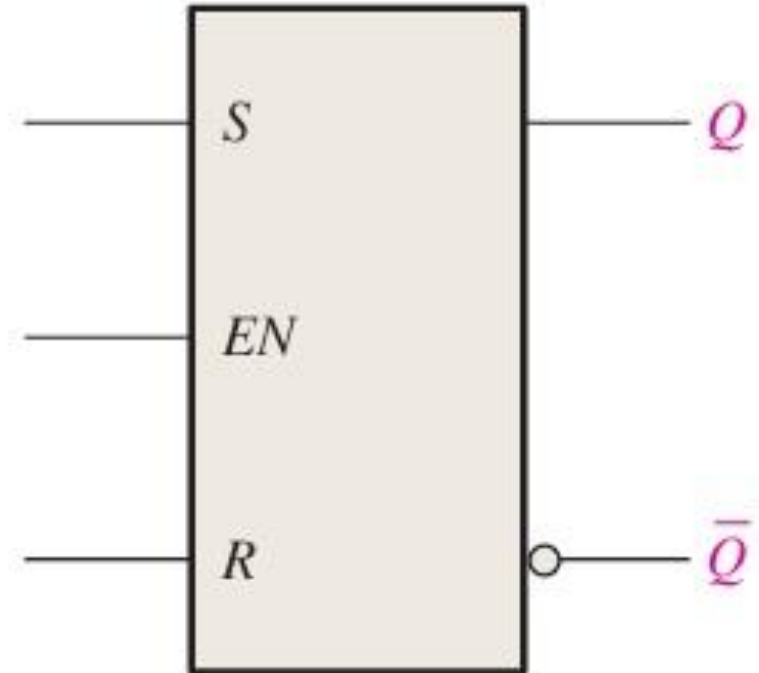
GATED S-R Latch

- The gated S-R Latch adds two NAND gates at the front of a basic S-R latch.
- It adds an Enable (EN) input that acts as a “gatekeeper”.
- This Latch only looks at the inputs when the gate is open ($EN = 1$).

SYMBOL And DIAGRAM of Gated S-R Latch



(a) Logic diagram



(b) Logic symbol

LOGIC:

If $EN = 0$:

The Latch is “Locked”. No matter what the values of S & R are, the output stays the same.

If $EN = 1$:

The Latch behaves like a standard S-R latch.

FLAW:

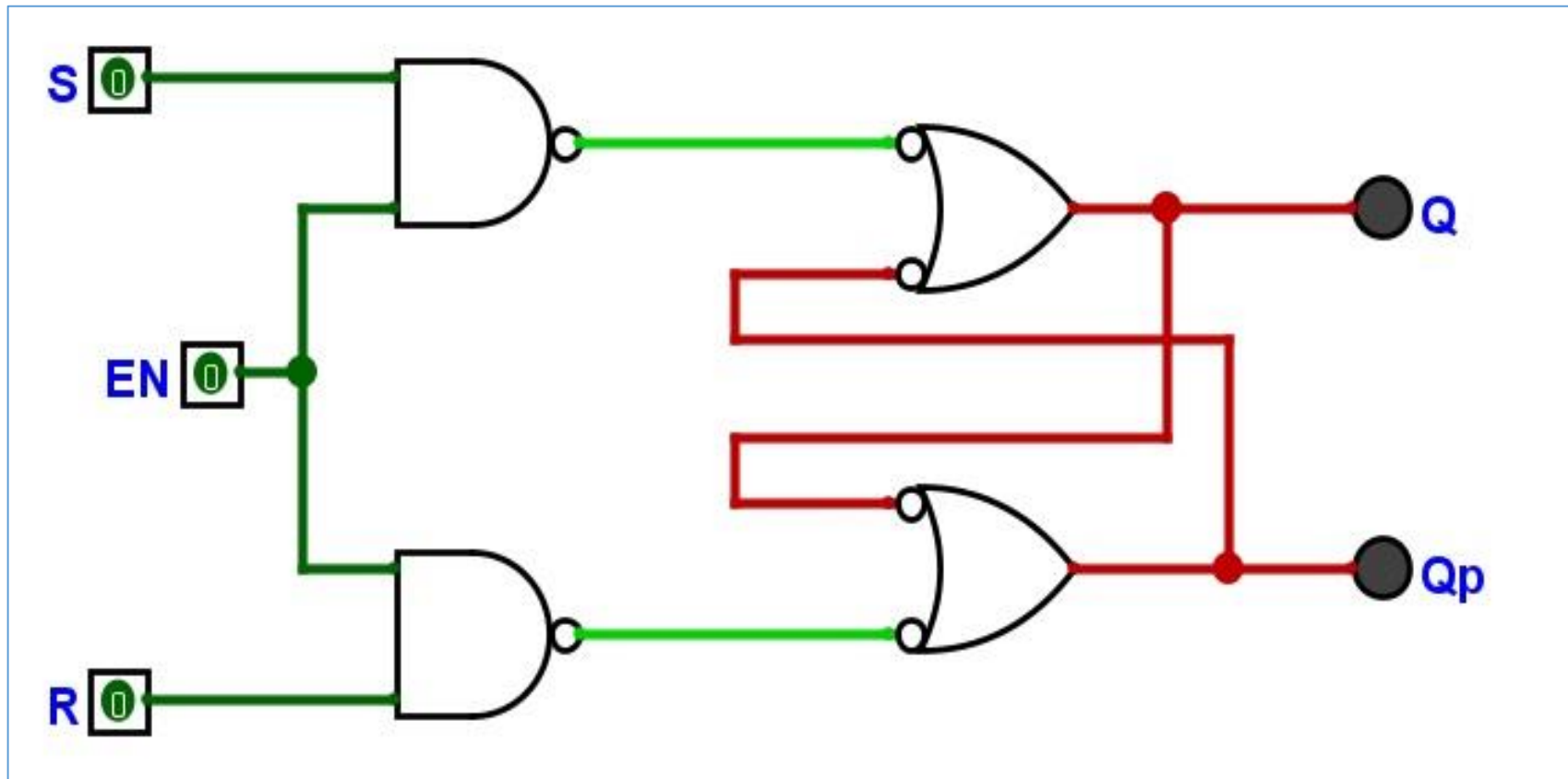
Even with the gate, the invalid state ($S=1$, $R=1$, $EN=1$) still exists.

OPERATIONS of Gated S-R Latch

$S = 0$

$EN = 0$

$R = 0$



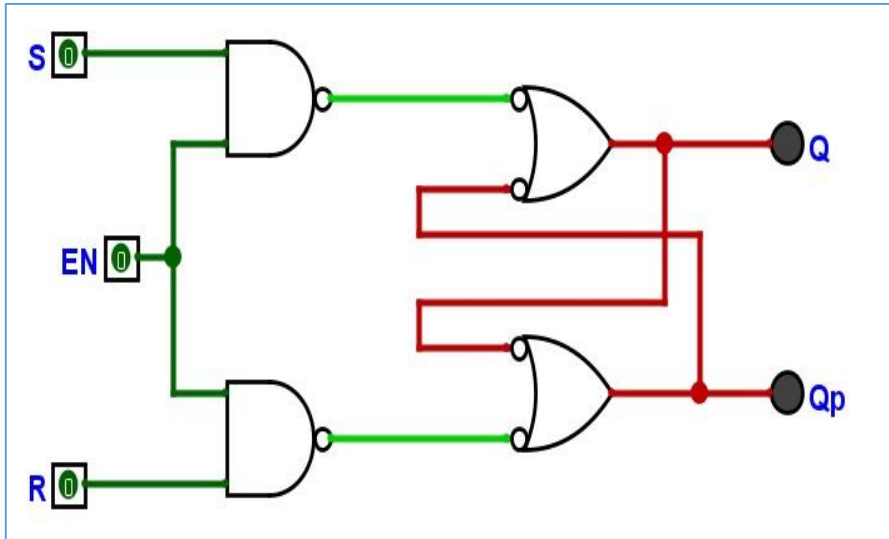
OPERATIONS of Gated S-R Latch

In all 4 cases, No effect on Output because **EN=0**

S = 0

EN = 0

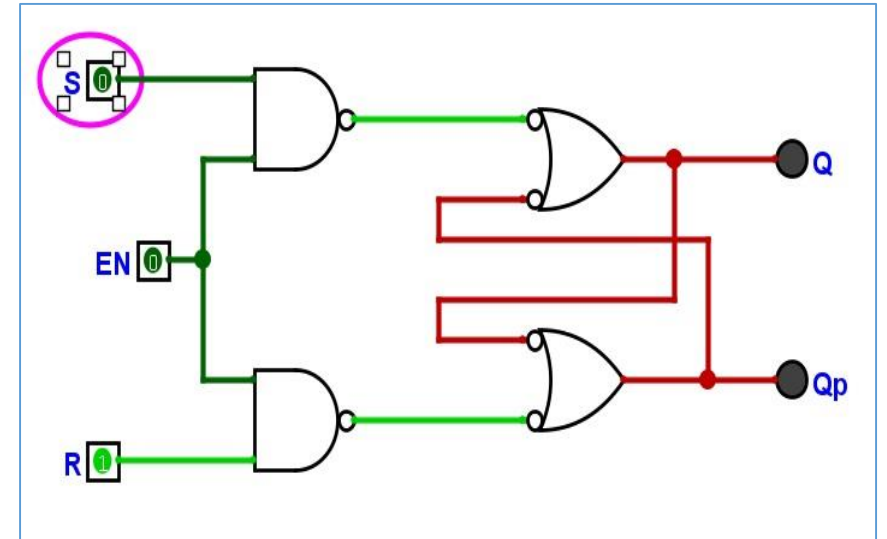
R = 0



S = 0

EN = 0

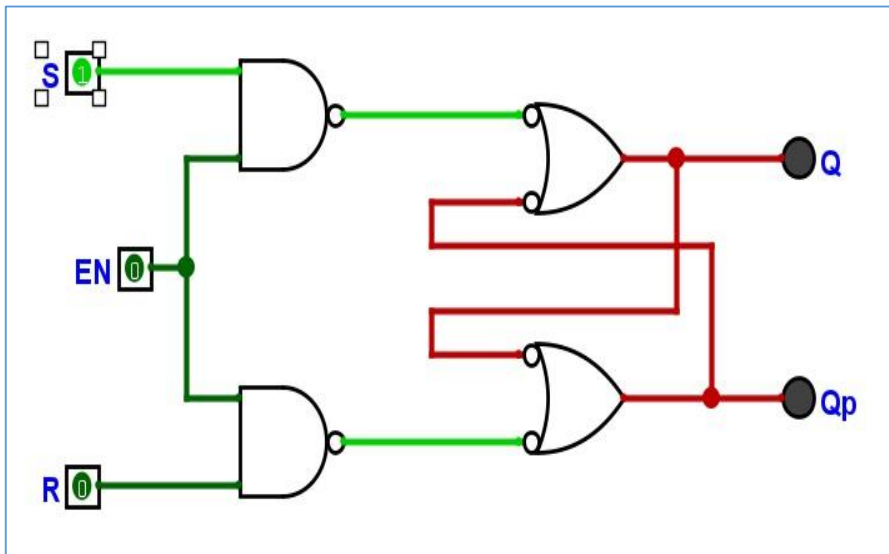
R = 1



S = 1

EN = 0

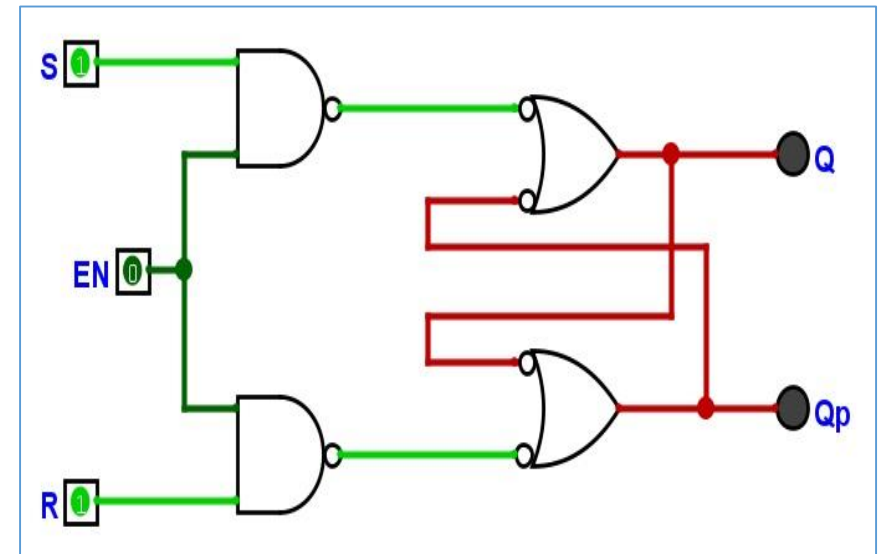
R = 0



S = 1

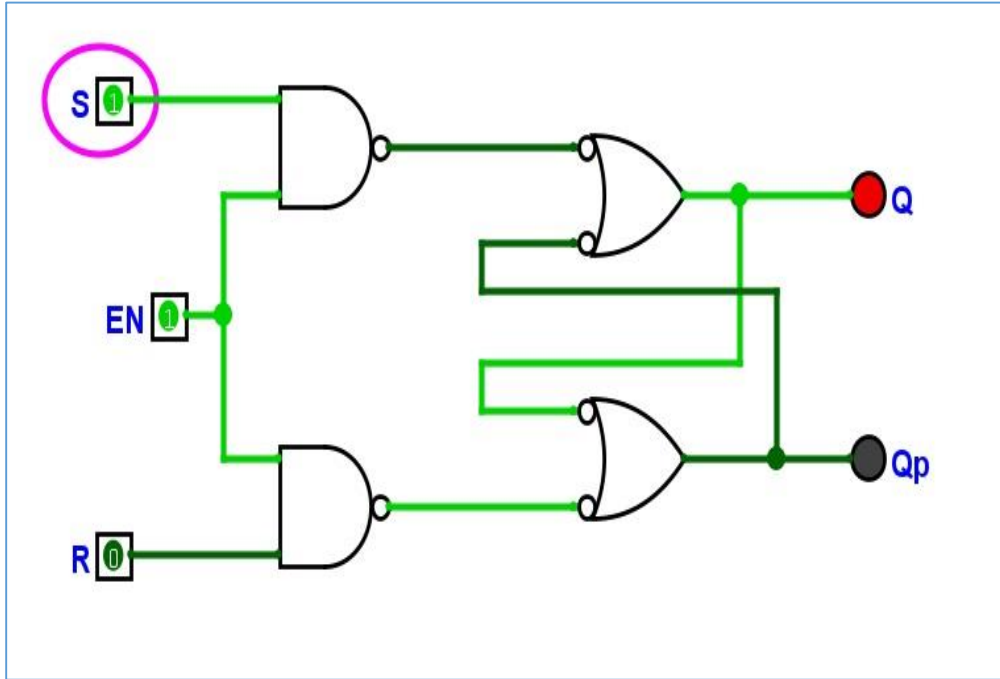
EN = 0

R = 1



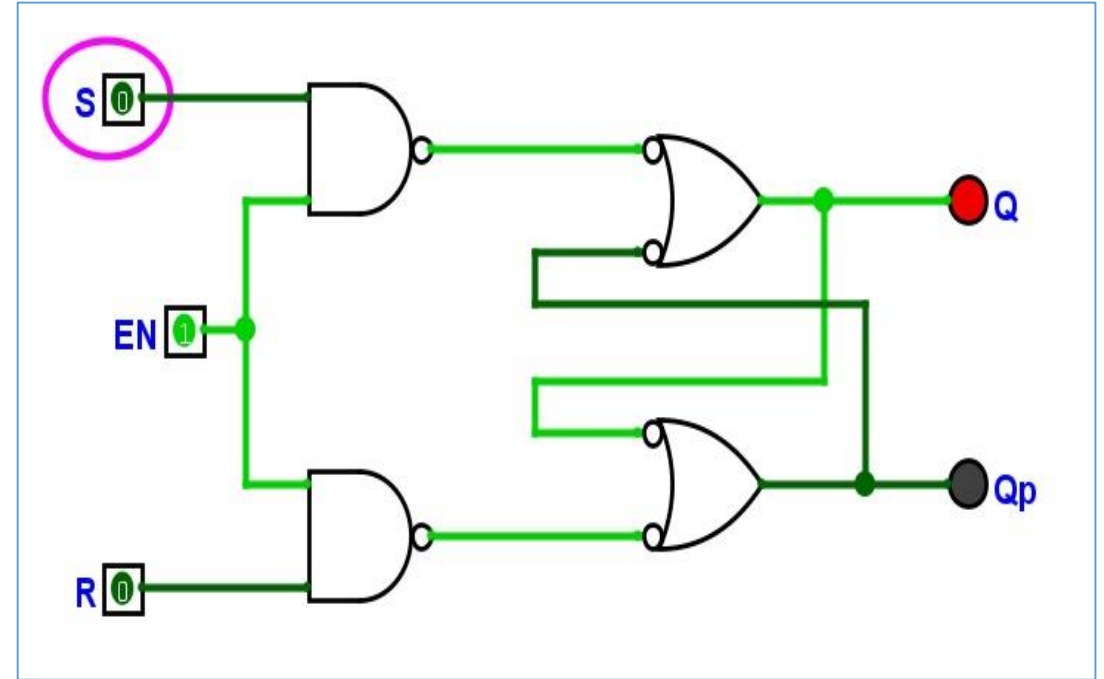
Logisim Screen Capture

OPERATIONS of Gated S-R Latch



$S = 1, EN = 1, R = 0$

$Q = 1, \bar{Q} = 0$

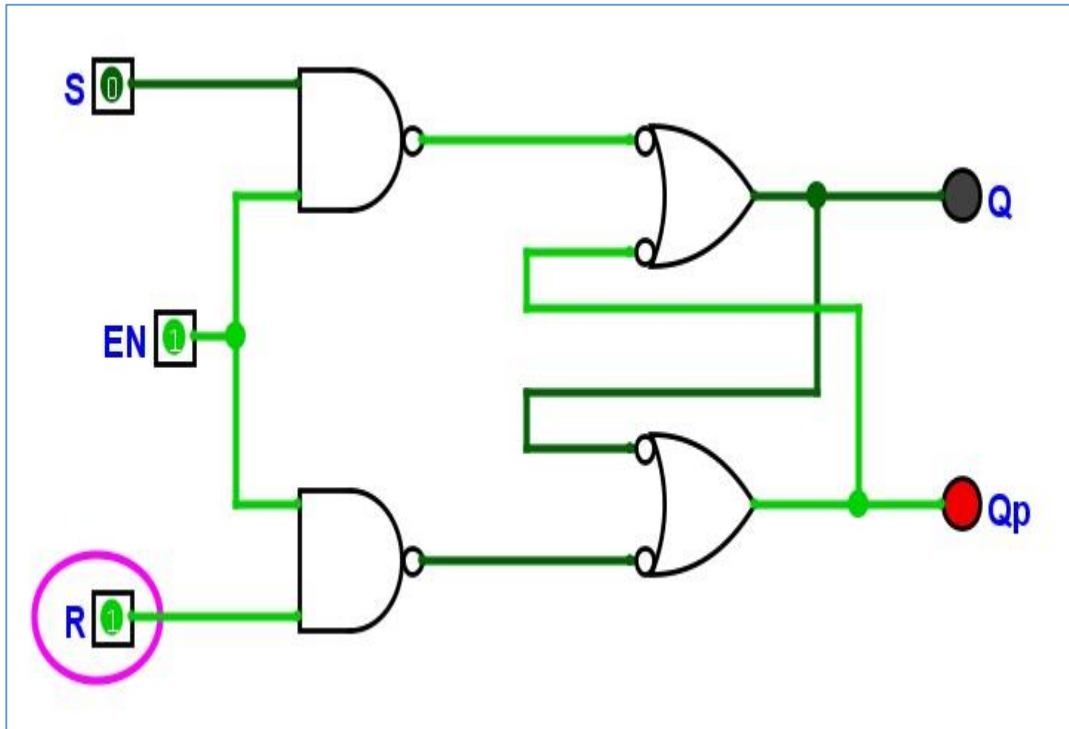


Input : $S = 0, EN = 1, R = 0$,

Output: $Q = 1, \bar{Q} = 0$

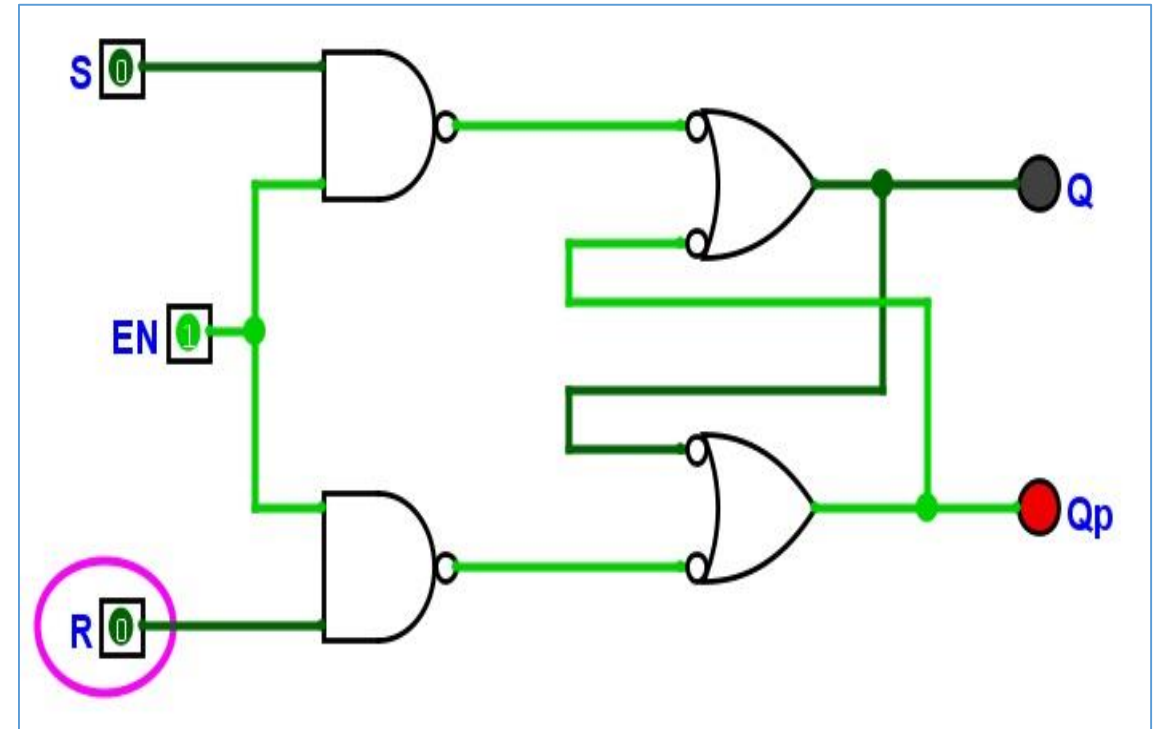
State retained even after S goes LOW

OPERATIONS of Gated S-R Latch



Input : $S = 0, EN = 1, R = 1$,
Output: $Q = 0, \bar{Q} = 1$

State Changed when R goes HIGH



Input : $S = 0, EN = 1, R = 0$,
Output: $Q = 1, \bar{Q} = 0$

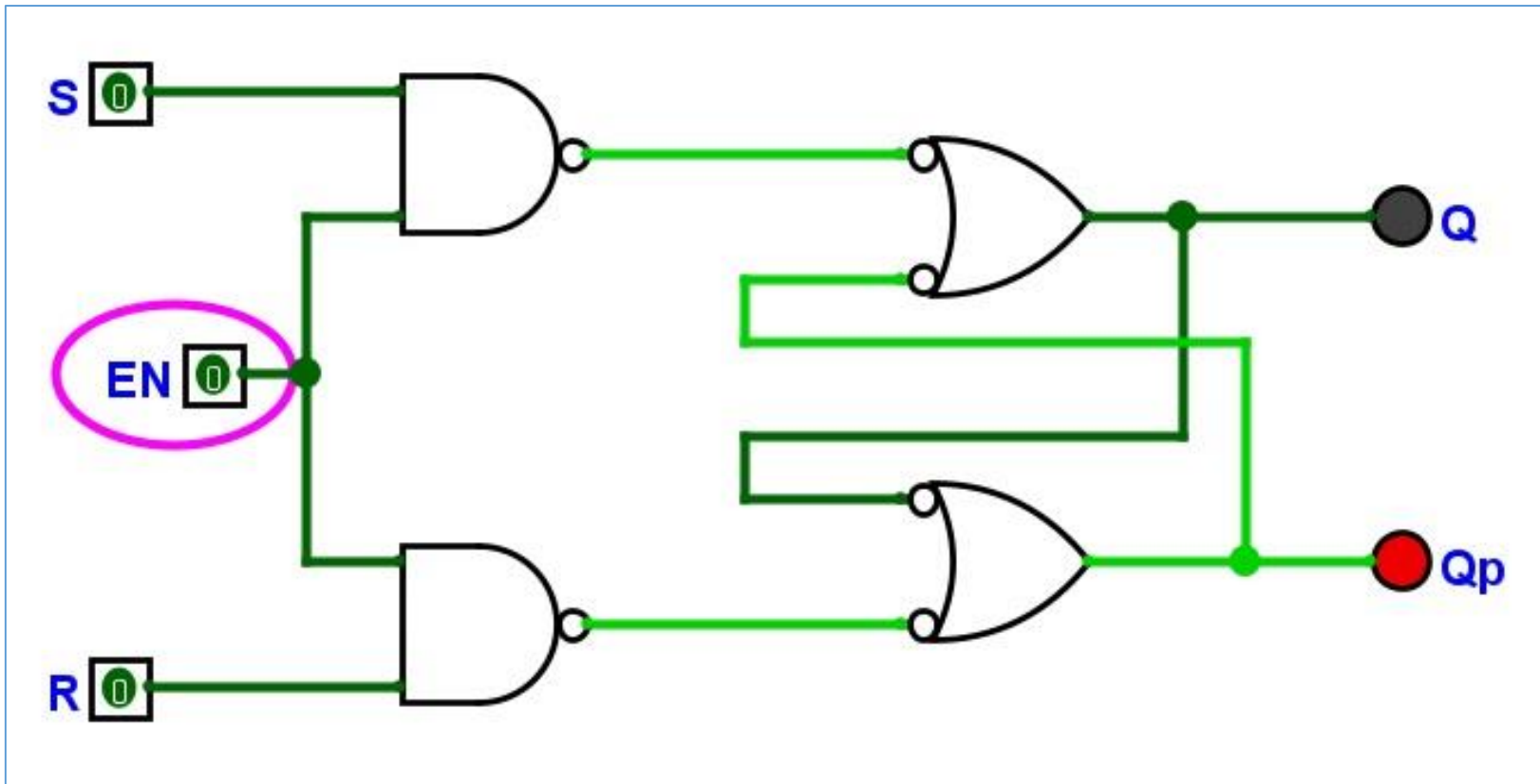
State Retained even after R goes back LOW

OPERATIONS of Gated S-R Latch

Input : $S = 0, EN = 1, R = 0,$

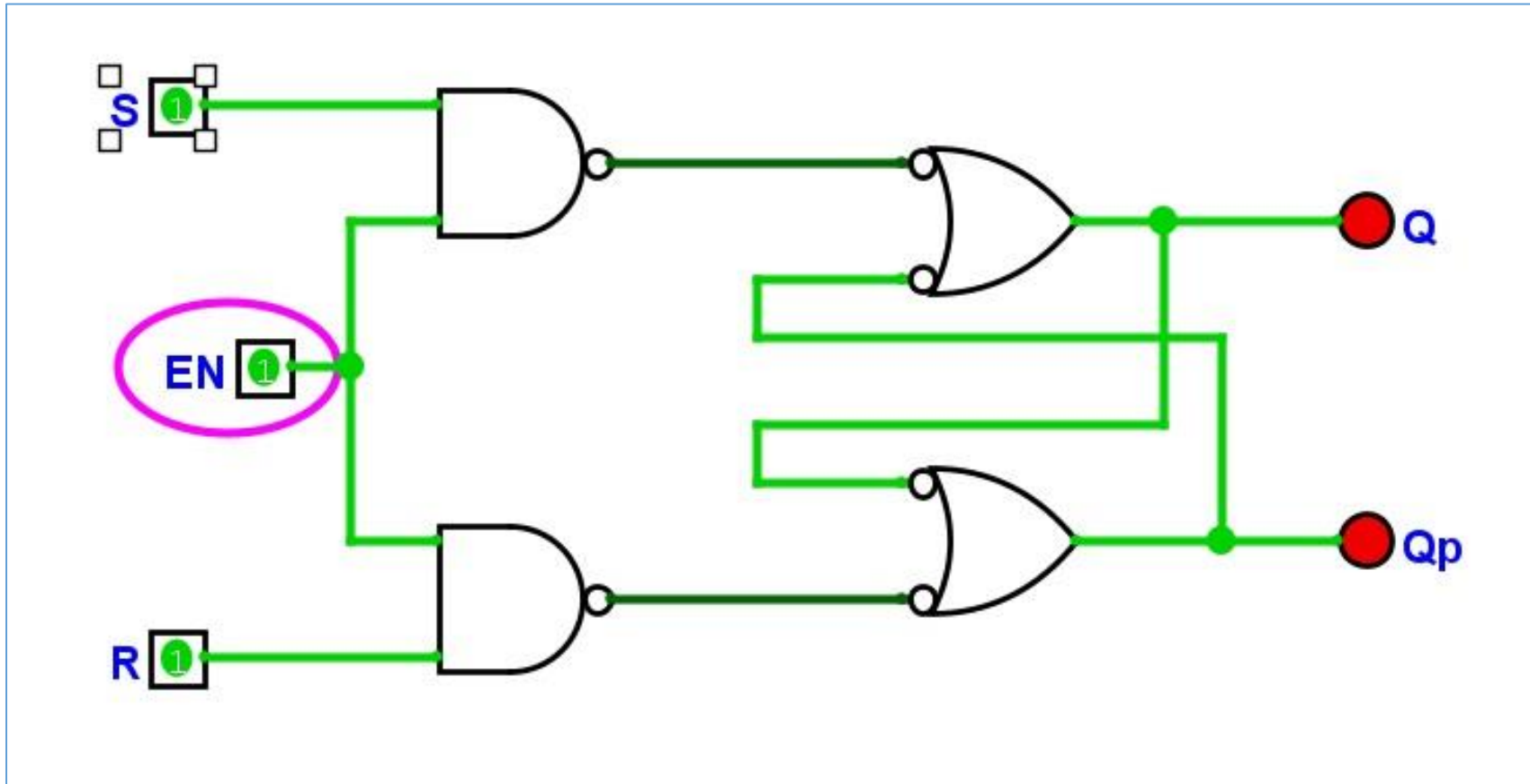
Output: $Q = 1, \bar{Q} = 0$

State Retained even after EN goes back LOW

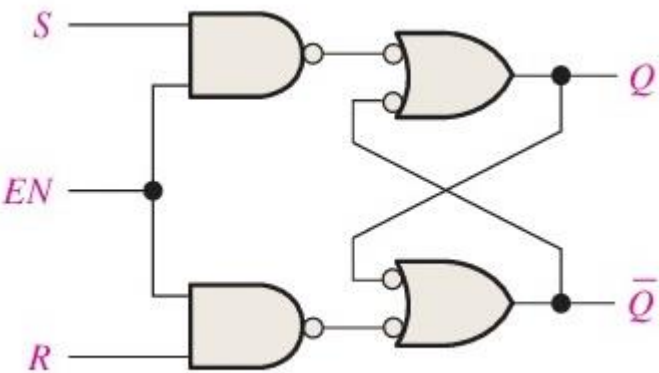
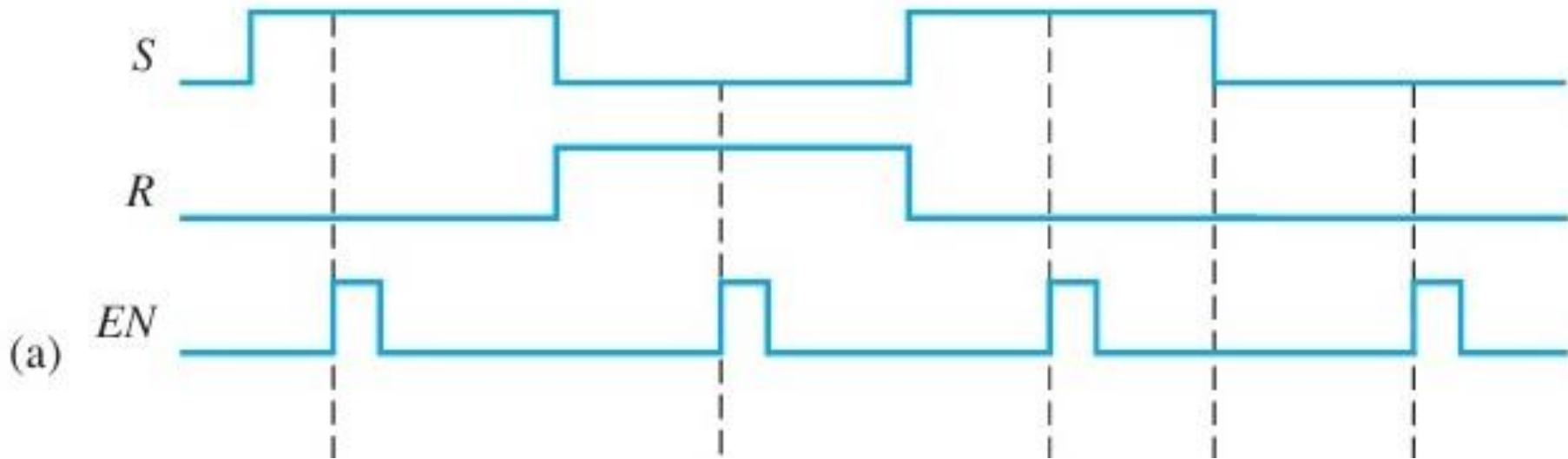


INVALID STATE

Input : $S = 1, EN = 1, R = 1,$
 Output: $Q = 1, \bar{Q} = 1$



Determine the Q output waveform if the inputs shown in Figure 7–9(a) are applied to a gated S-R latch that is initially RESET.



EXAMPLE 7-2

Determine the Q output waveform if the inputs shown in Figure 7-9(a) are applied to a gated S-R latch that is initially RESET.

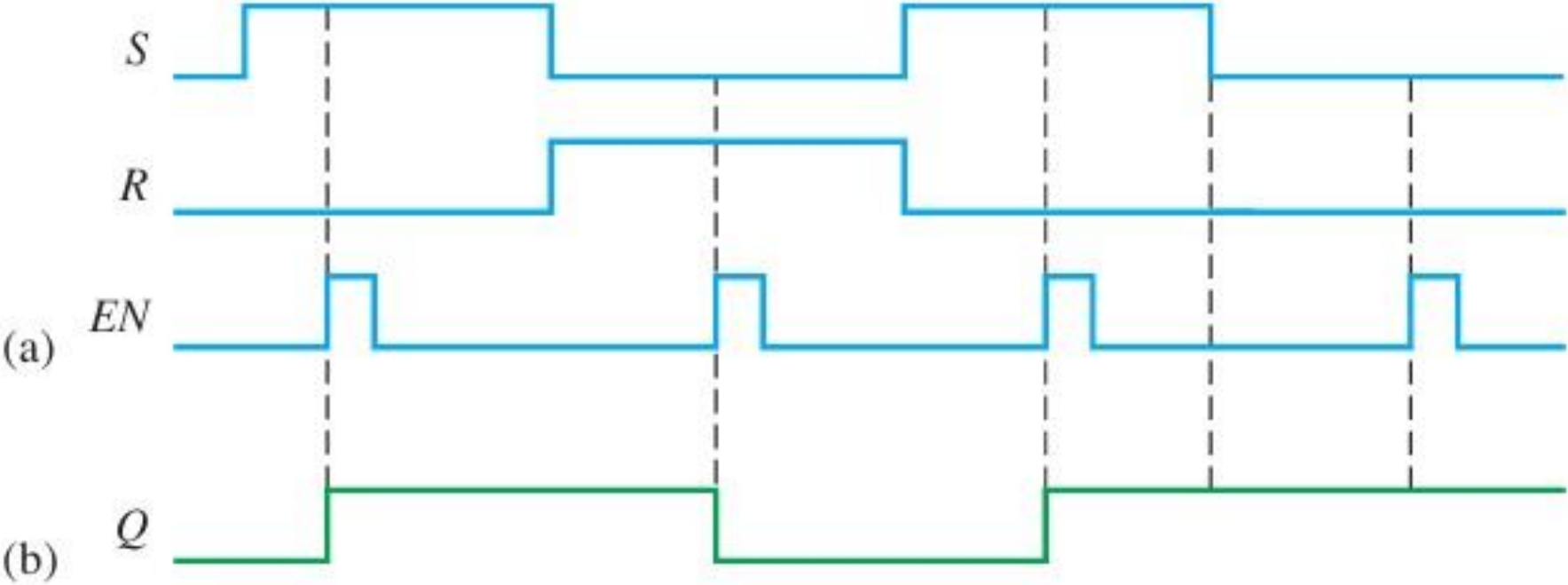
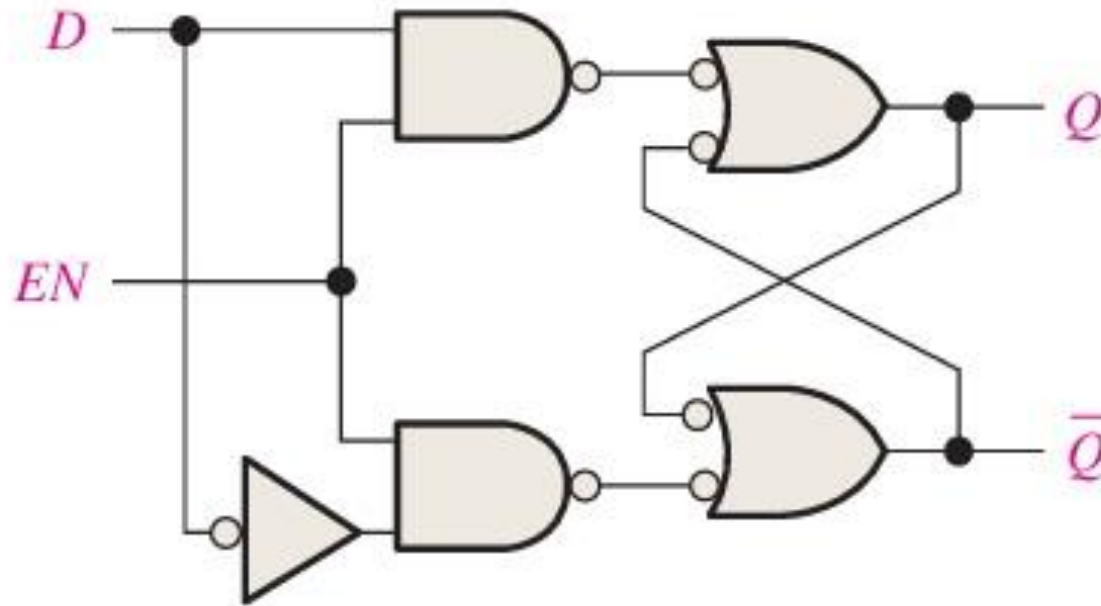


FIGURE 7-9

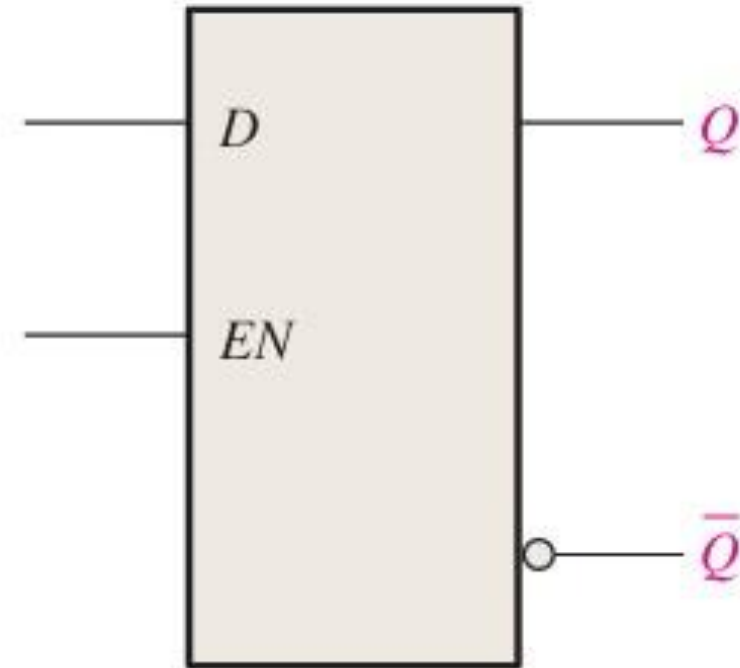
GATED D Latch

- It is the most common type of latch.
- It simplifies the gated S-R latch by using a single Data (D) input and an inverter.
- This inverter ensures that the inputs **S** & **R** are always complement of each other.

SYMBOL And DIAGRAM of Gated D Latch



(a) Logic diagram



(b) Logic symbol

LOGIC:

If $EN = 0$:

Output is “Latched” (Held)

If $EN = 1$:

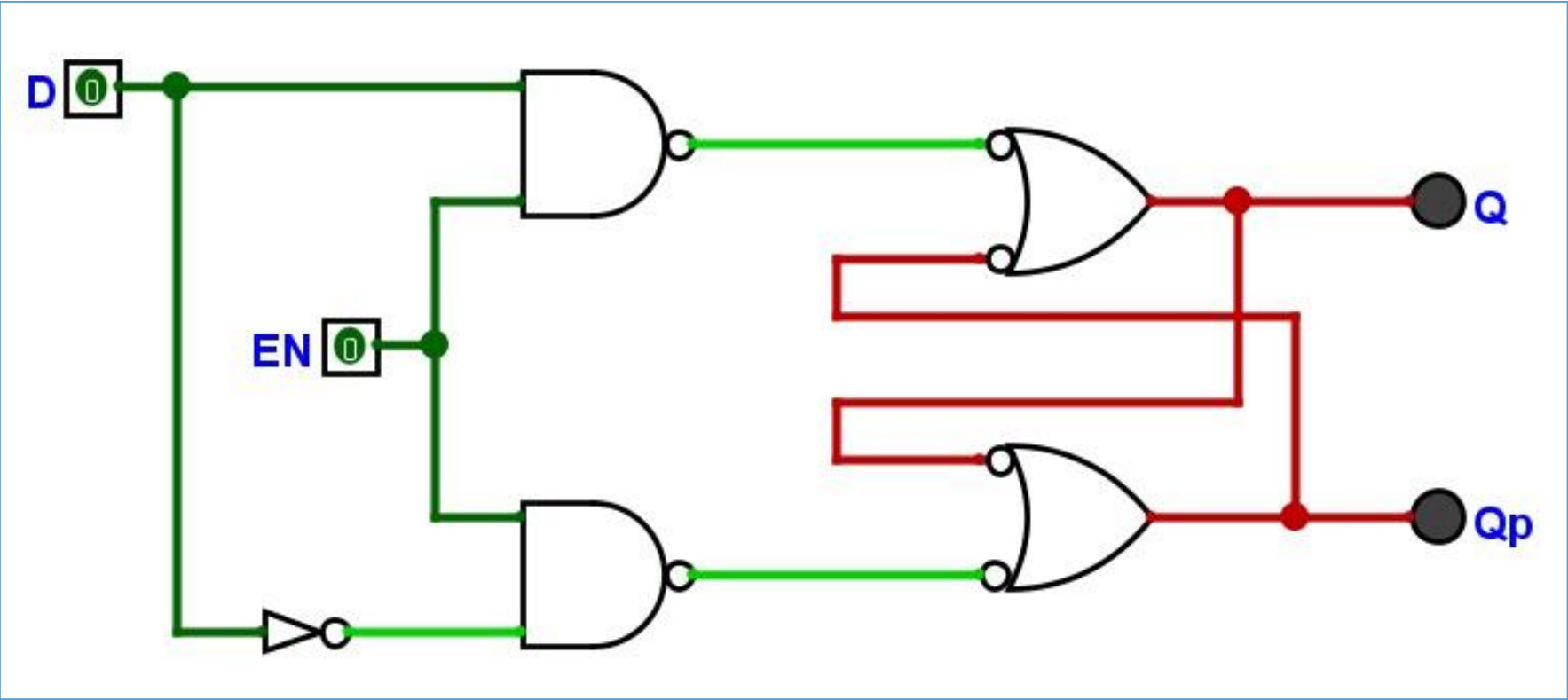
The output Q follows the input D.

If D is 1, Q is 1.

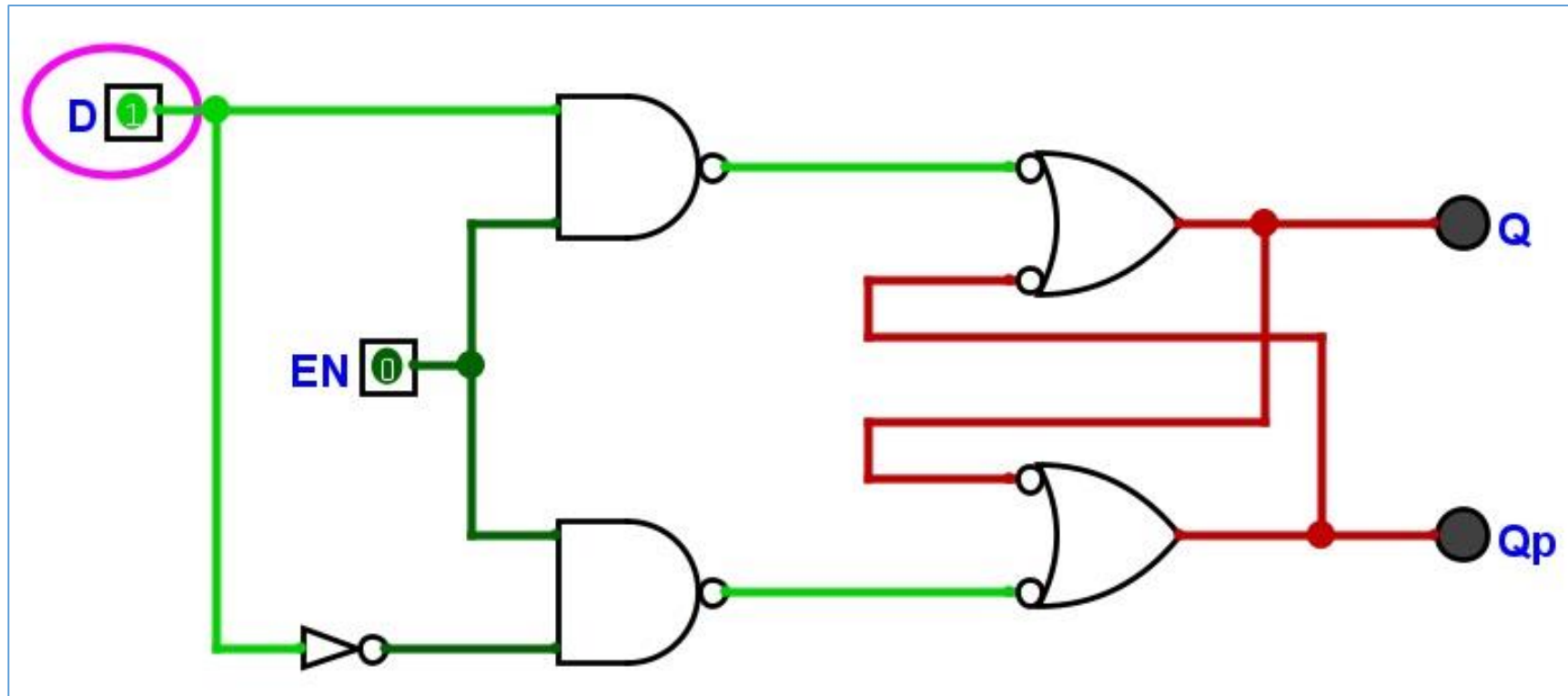
If D is 0, Q is 0.

OPERATIONS of Gated D Latch

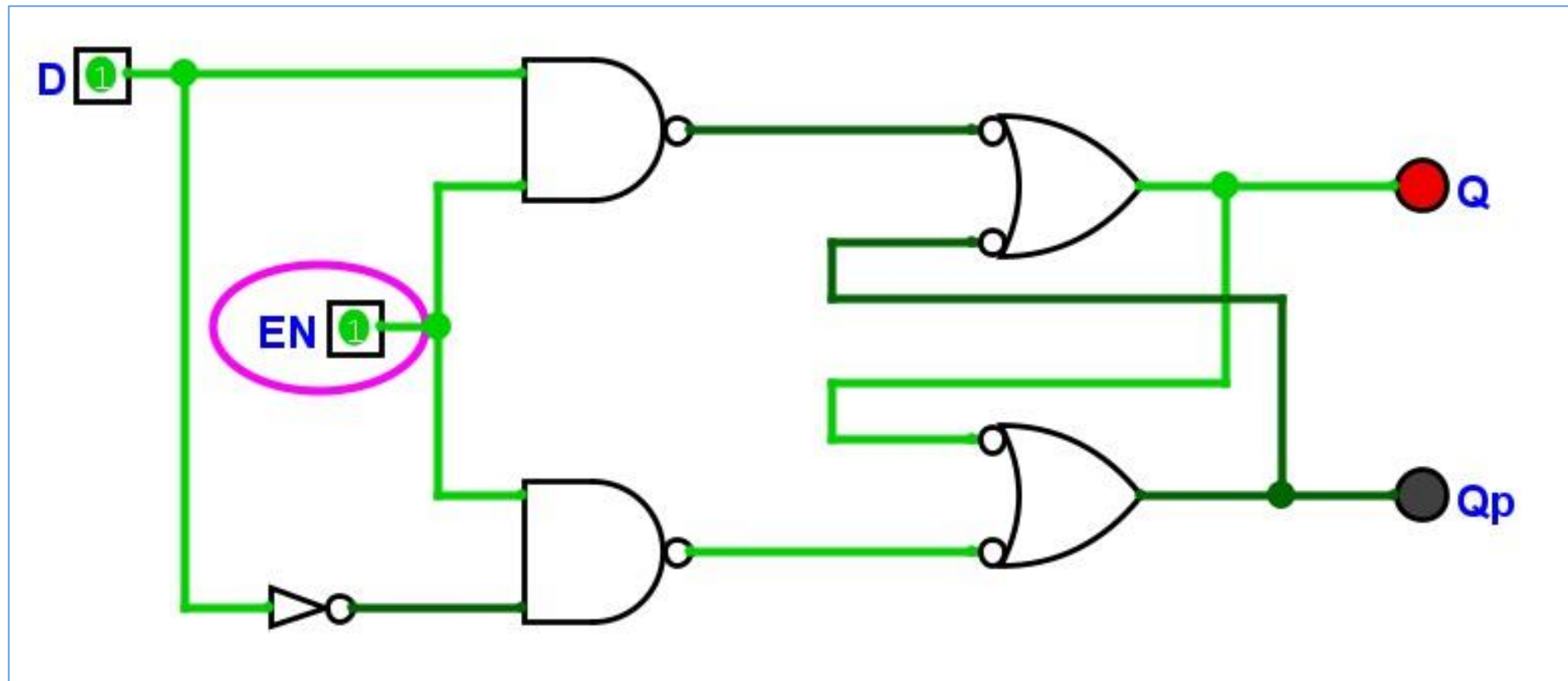
Latch is UNSET when EN = 0



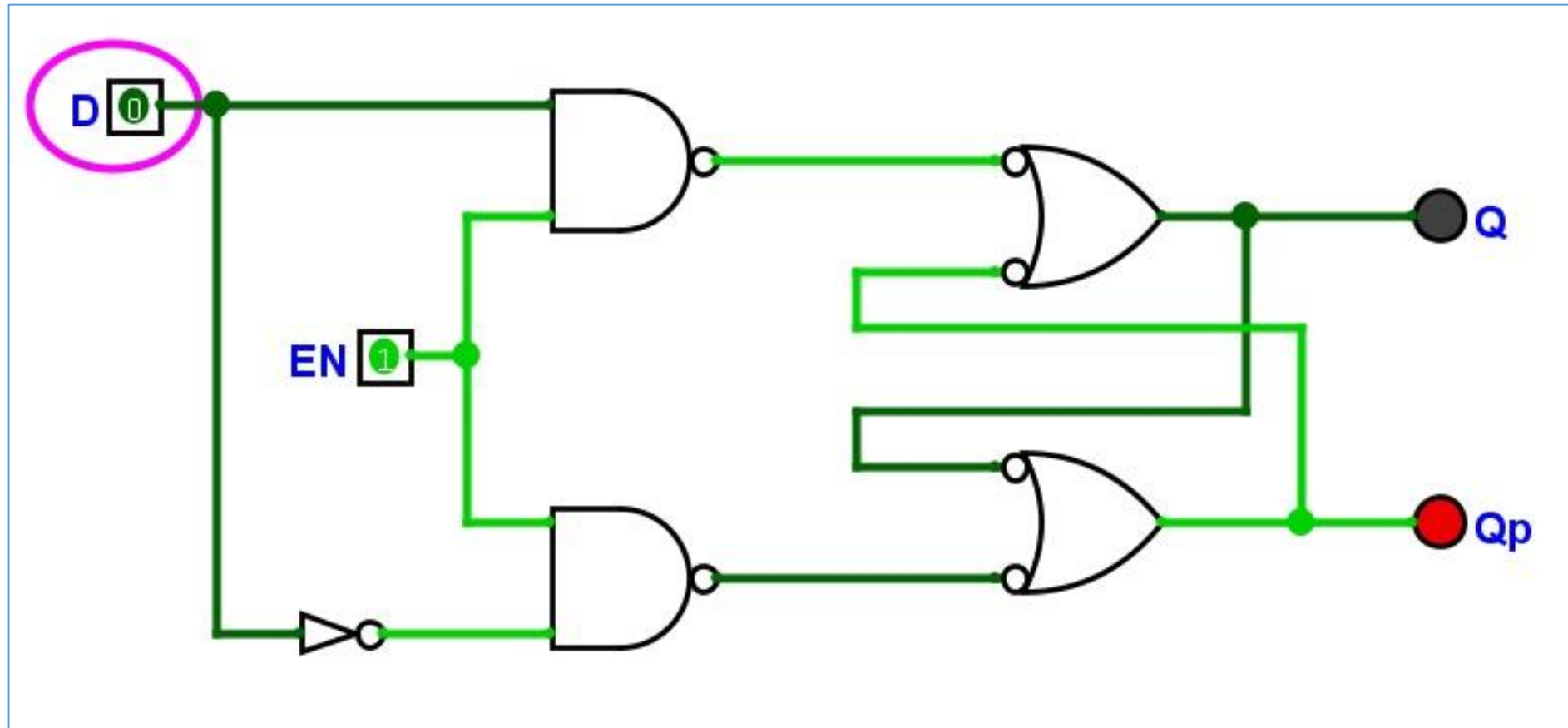
Latch remains UNSET even after $D = 1$, because $EN = 0$



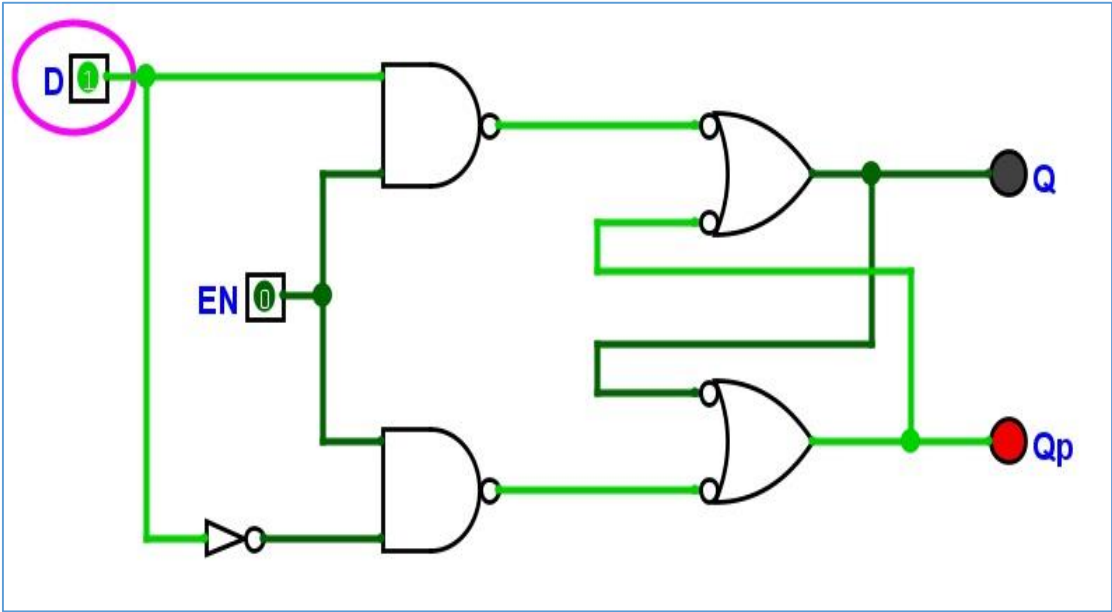
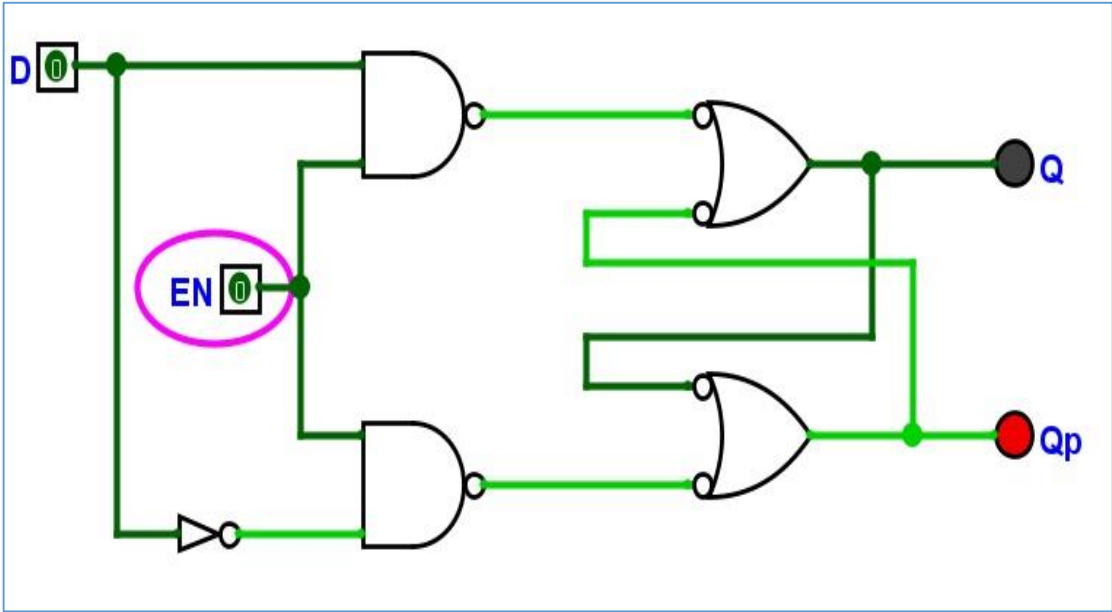
Latch will SET when both D is HIGH and EN is HIGH



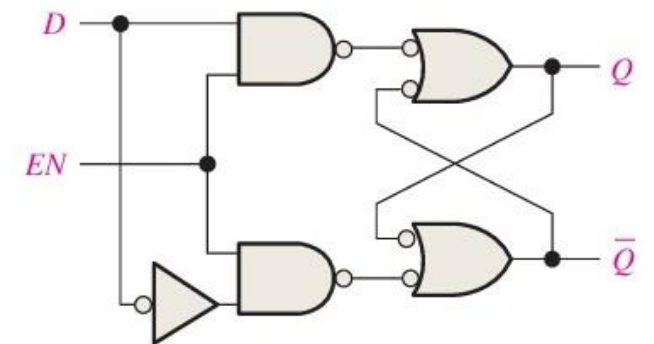
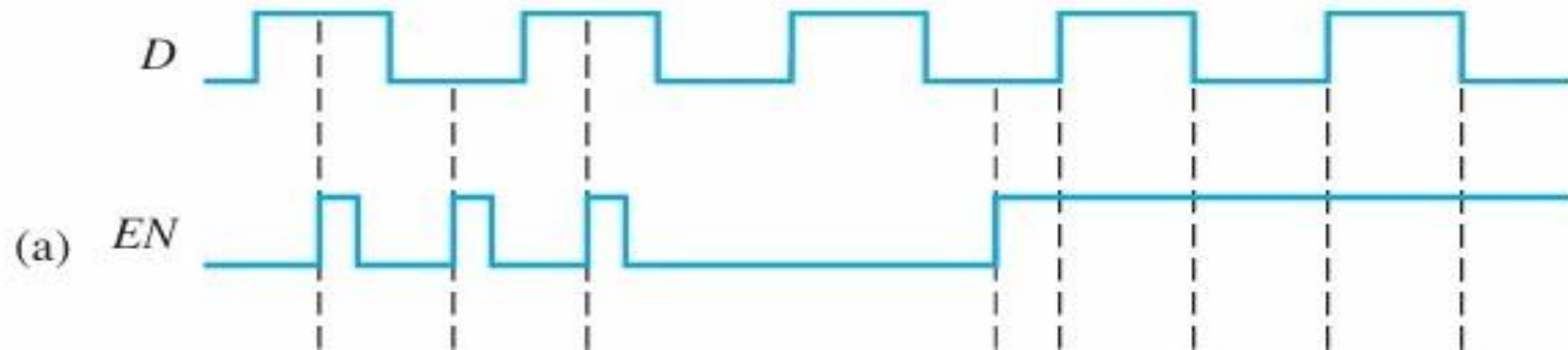
Latch will RESET when D is LOW and EN is HIGH



State Retained even after EN goes LOW, irrespective of D value

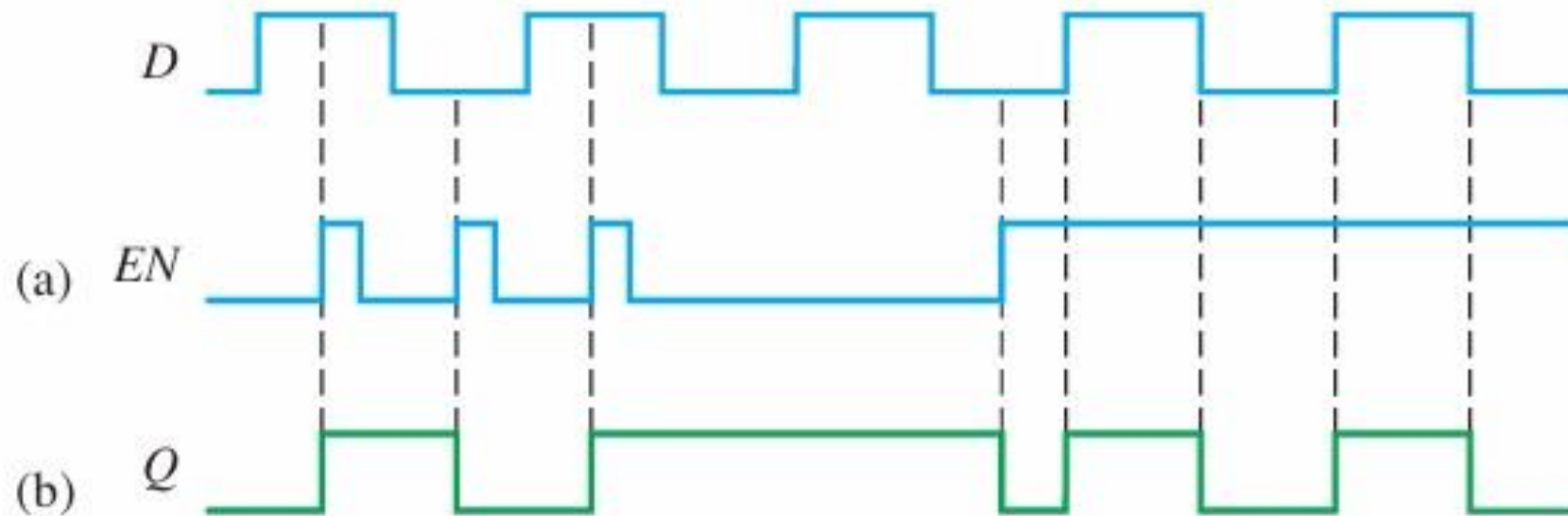


Determine the Q output waveform if the inputs shown in Figure 7–11(a) are applied to a gated D latch, which is initially RESET.



EXAMPLE 7-3

Determine the Q output waveform if the inputs shown in Figure 7-11(a) are applied to a gated D latch, which is initially RESET.

**FIGURE 7-11**

SUMMARY

There are two types of gated latches.

1. Gated S-R Latch
2. Gated D Latch

WHEN TO USE *WHICH* ?

GATED S-R:

It is used for Event-Driven Logic.

Sometimes there are two completely different parts of a machine controlling its states.

For Example;

A “low-pressure” sensor might trigger the SET (turn on a pump), while a “High pressure” sensor trigger the RESET (turn off the pump).

These are two independent signal.

GATED D:

It is used for data storage.

For example;

In a computer, we usually want to save a specific value (a 0 or a 1) at a specific time.

D Latch is fit for this.

Thank You