Flip-Flops

Digital Logic Design (CC131)

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Flip-Flops

- A Flip-flop is a fundamental building block of Sequential Logic circuits.
- It is a Synchronous bistable multivibrator which means it has two stable states (represented as 0 and 1).
- Synchronous means it acts with respect to another object, called Clock.
- It can store One bit of digital data.
- The output of a flip-flop depends on both its current inputs and its previous state.

Flip-Flops

- The Clock (CLK) input is the most important control signal which distinguishes it from a Latch.

- The clock has a special component called Edge-Detector, which makes sure that the Flip-flop only looks at the data input at the specific transition of the pulse (rising edge or falling edge).

- Flip-flops are edge-triggered or edge-sensitive devices.

Flip-Flops

- The edge-triggered flip-flop changes its state only at the positive edge (rising edge) or at the negative edge (falling edge) of the clock pulse.

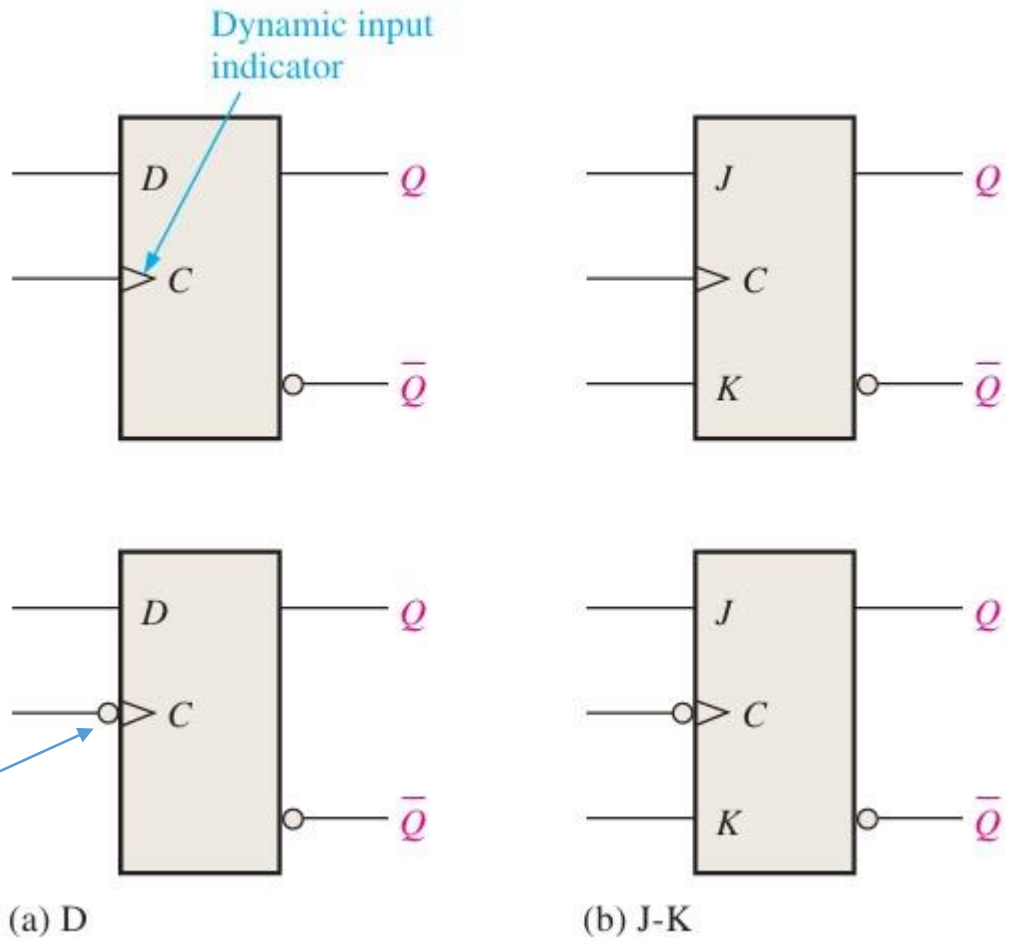
- It looks on the input only when the specified (positive edge or negative edge) clock transition occurs and flips its state accordingly.

- A small triangle at the Clock input (C), in its symbol, is called Dynamic input indicator and this is the identification mark of an edge-triggered flip-flop.

SYMBOLS

Positive Edge-Triggered Flip-Flops

Negative Edge-Triggered Flip-Flops



APPLICATIONS of Flip-Flops

Data Storage: basic unit of memory in registers and Cache

Counters: counts pulses or events in digital systems

State Machines: stores “current state” in complex controllers and processors

TYPES of Flip-Flops

Two types are discussed.

1. D Flip-flop
2. J-K Flip-flop

D Flip-Flops

- The Data flip-flop has an input D which is reflected on the output Q only on the triggering edge of the clock pulse.
- D is called synchronous input.

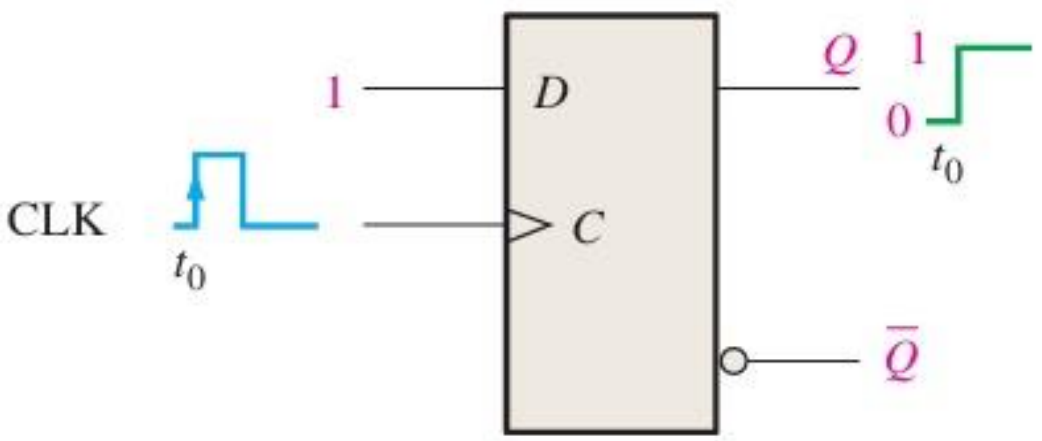
- **SET State**:

  When D is HIGH, the Q also goes HIGH on the triggering edge of the clock pulse.

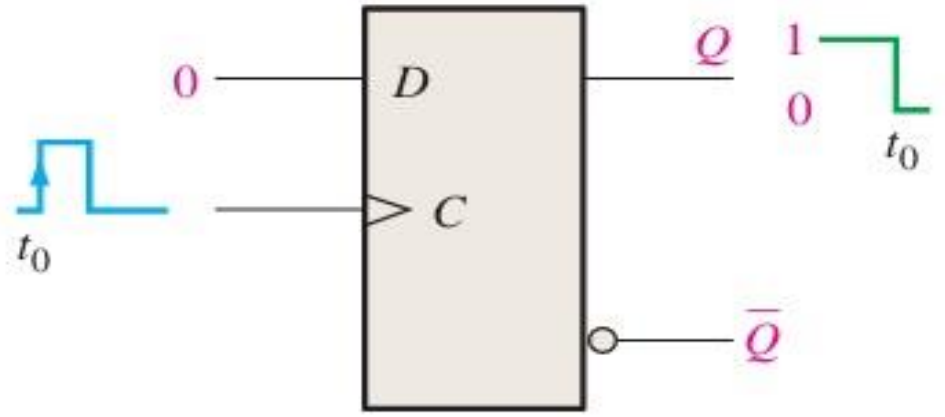
- **RESET State**:

  When D is LOW, the Q also goes LOW on the triggering edge of the clock pulse.

Operation of a Positive edge-triggered D Flip-Flop.



(a) $D = 1$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b) $D = 0$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

REMEMBER:

- Q follows D at the triggering edge of the clock pulse.
- The flip-flop cannot change its state except on the triggering edge of the clock pulse.

D Flip-Flops

Truth table for a positive edge-triggered D flip-flop.

Inputs		Outputs		
D	CLK	Q	$\overline{Q}$	Comments
0	↑	0	1	RESET
1	↑	1	0	SET

↑ = clock transition LOW to HIGH

Example

Determine the Q and $\overline{Q}$ output waveforms of the flip-flop in Figure 7–15 for the D and CLK inputs in Figure 7–16(a). Assume that the positive edge-triggered flip-flop is initially RESET.

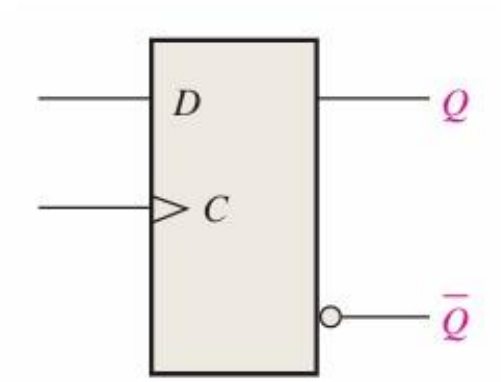


FIGURE 7–15

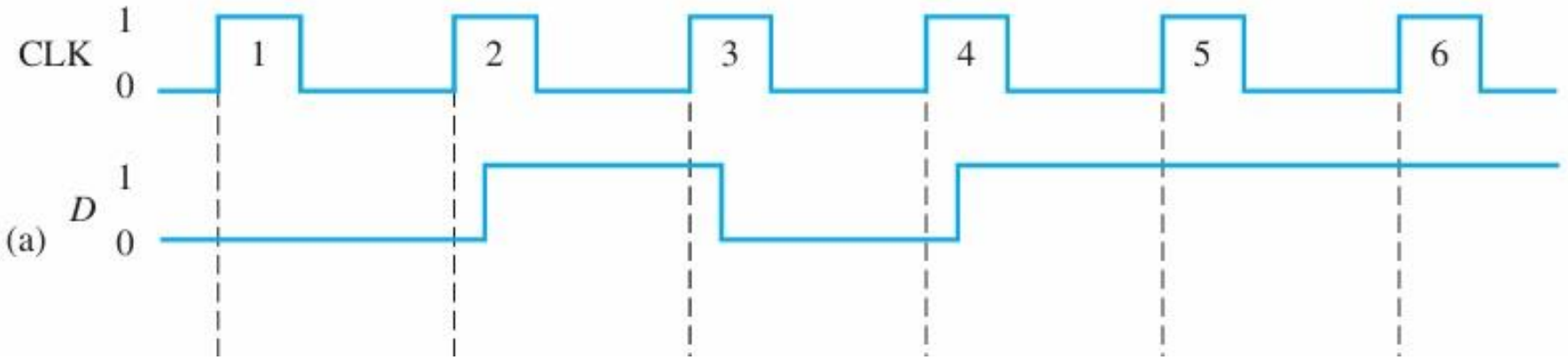


FIGURE 7–16

Solution

EXAMPLE 7–4

Determine the Q and $\overline{Q}$ output waveforms of the flip-flop in Figure 7–15 for the D and CLK inputs in Figure 7–16(a). Assume that the positive edge-triggered flip-flop is initially RESET.

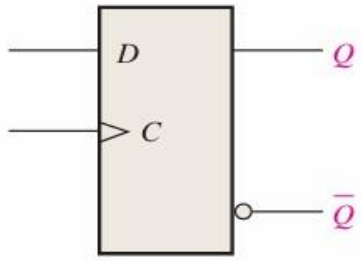


FIGURE 7–15

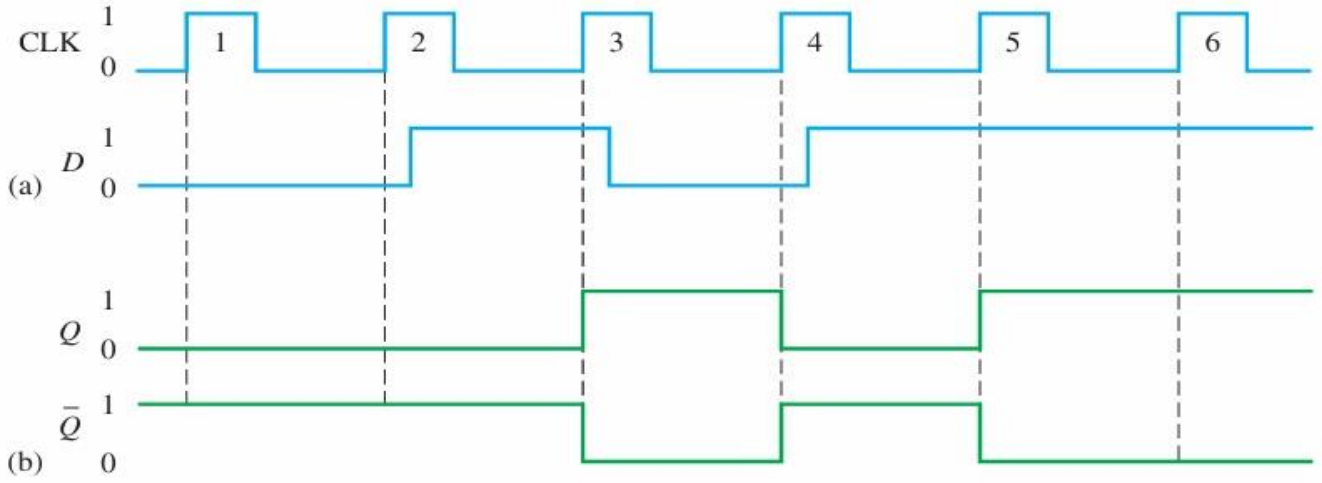


FIGURE 7–16

Solution

1. At clock pulse 1, D is LOW, so Q remains LOW (RESET).
2. At clock pulse 2, D is LOW, so Q remains LOW (RESET).
3. At clock pulse 3, D is HIGH, so Q goes HIGH (SET).
4. At clock pulse 4, D is LOW, so Q goes LOW (RESET).
5. At clock pulse 5, D is HIGH, so Q goes HIGH (SET).
6. At clock pulse 6, D is HIGH, so Q remains HIGH (SET).

Once Q is determined, $\overline{Q}$ is easily found since it is simply the complement of Q.

J-K Flip-Flops

- The J-K flip-flop has two synchronous inputs J and K.

- **SET State**:

  When J is HIGH and K is LOW,

  the Q goes HIGH on the triggering edge of the clock pulse.

- **RESET State**:

  When J is LOW and K is HIGH,

  the Q goes LOW on the triggering edge of the clock pulse

- **No Change State**:

  When both J and K are LOW,

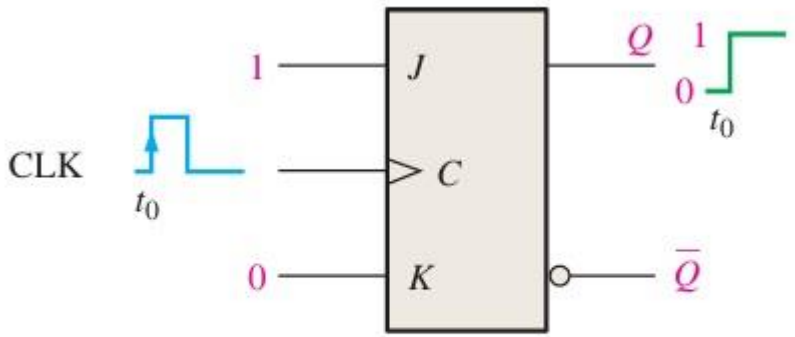
  the Output does not change from its previous state.

- **TOGGLE Mode**:

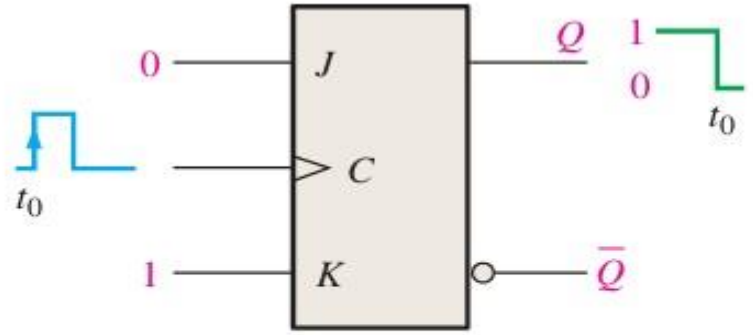
  When both J and K are HIGH,

  the flip-flop changes state.

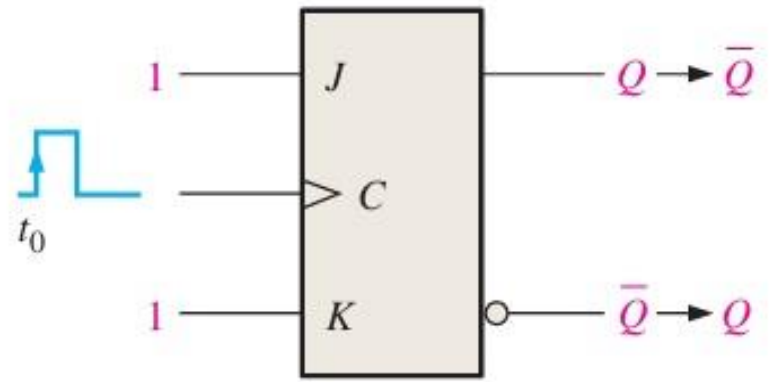
Operation of a Positive edge-triggered J-K Flip-Flop.



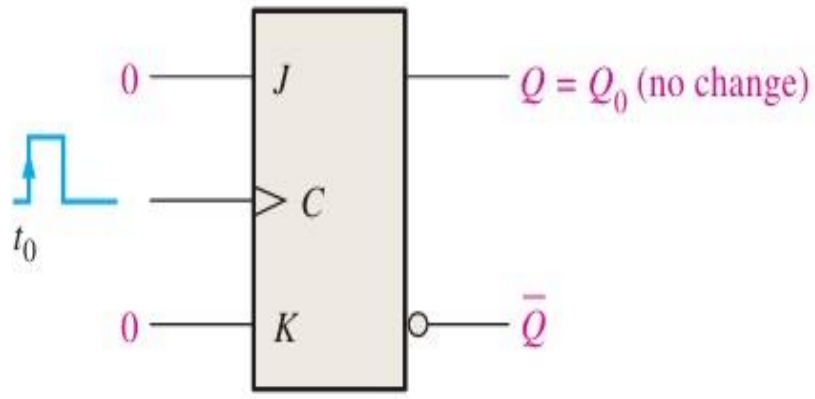
(a) $J = 1$, $K = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b) $J = 0$, $K = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)



(c) $J = 1$, $K = 1$ flip-flop changes state (toggle).



(d) $J = 0$, $K = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

J-K Flip-Flops

Truth table for a positive edge-triggered J-K flip-flop.

Inputs			Outputs		
J	K	CLK	Q	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

↑ = clock transition LOW to HIGH

Q_0 = output level prior to clock transition

Example

The waveforms in Figure 7–18(a) are applied to the *J*, *K*, and clock inputs as indicated. Determine the *Q* output, assuming that the flip-flop is initially RESET.

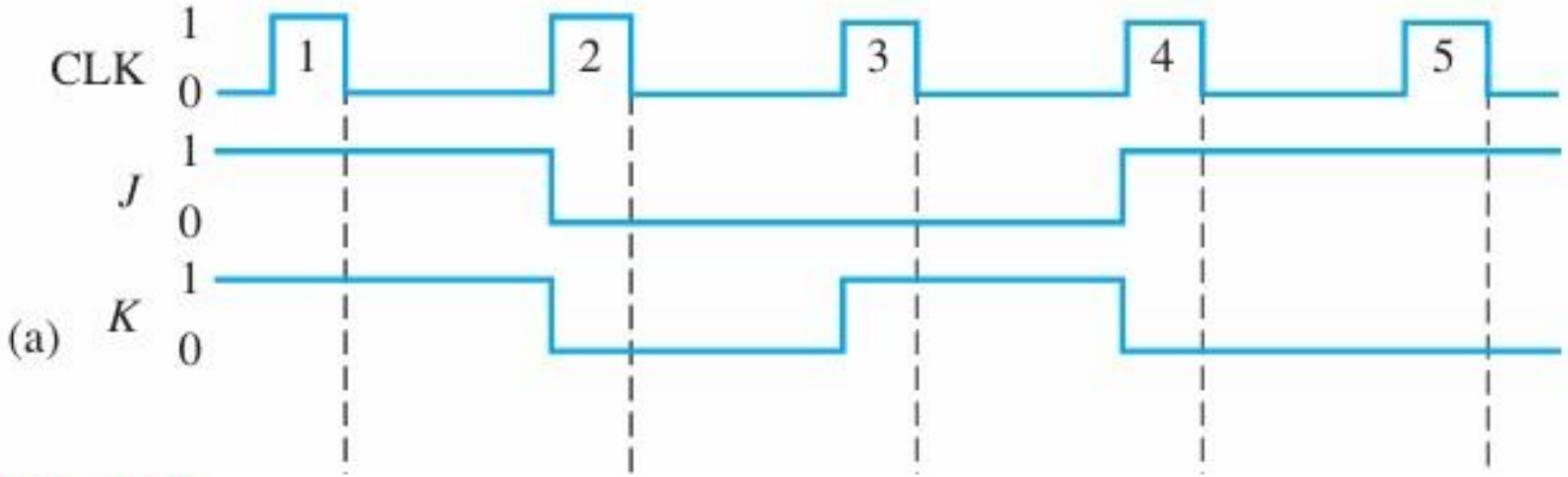
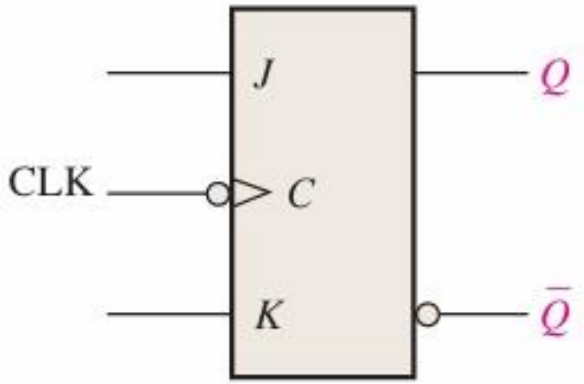


FIGURE 7–18



Solution

EXAMPLE 7–5

The waveforms in Figure 7–18(a) are applied to the *J*, *K*, and clock inputs as indicated. Determine the *Q* output, assuming that the flip-flop is initially RESET.

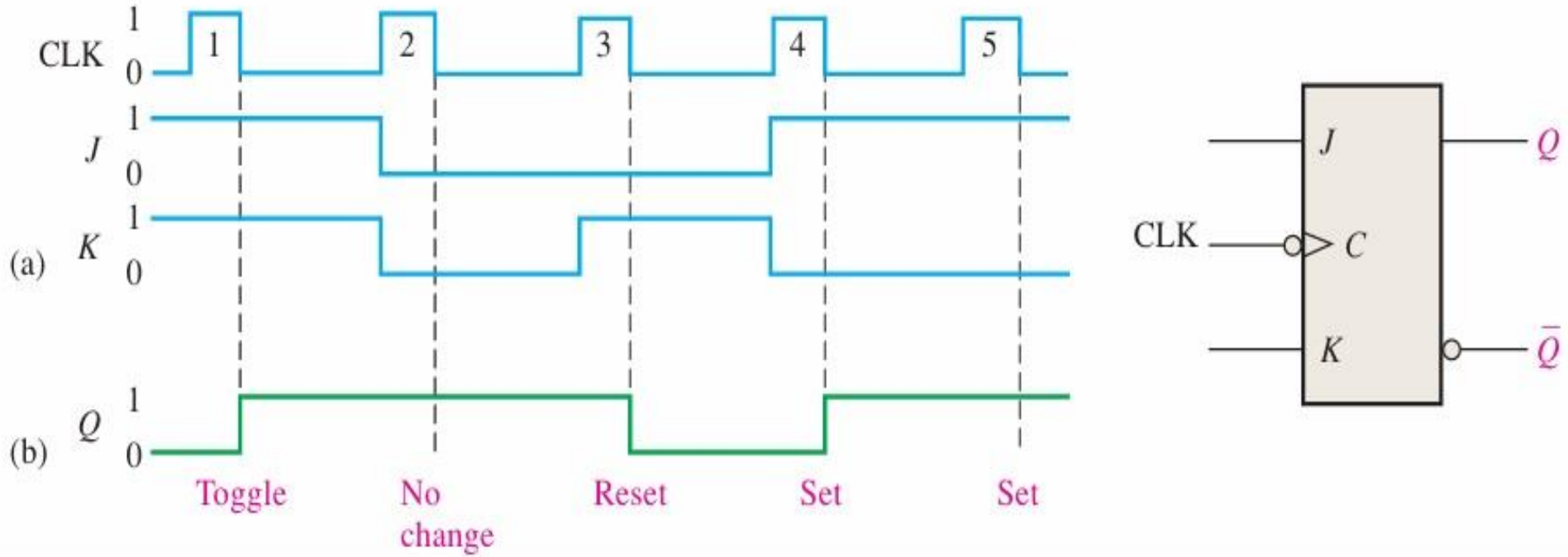


FIGURE 7–18

J-K Flip-Flops

Solution

EXAMPLE 7–5

The waveforms in Figure 7–18(a) are applied to the *J*, *K*, and clock inputs as indicated. Determine the *Q* output, assuming that the flip-flop is initially RESET.

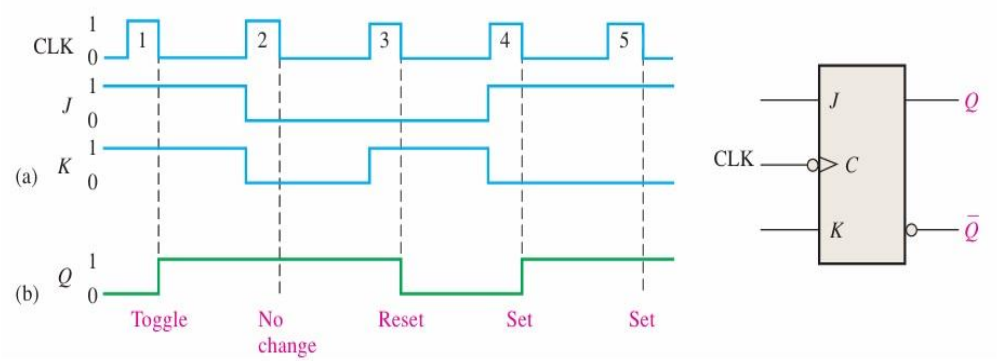


FIGURE 7–18

Solution

Since this is a negative edge-triggered flip-flop, as indicated by the "bubble" at the clock input, the *Q* output will change only on the negative-going edge of the clock pulse.

1. At the first clock pulse, both *J* and *K* are HIGH; and because this is a toggle condition, *Q* goes HIGH.
2. At clock pulse 2, a no-change condition exists on the inputs, keeping *Q* at a HIGH level.
3. When clock pulse 3 occurs, *J* is LOW and *K* is HIGH, resulting in a RESET condition; *Q* goes LOW.
4. At clock pulse 4, *J* is HIGH and *K* is LOW, resulting in a SET condition; *Q* goes HIGH.
5. A SET condition still exists on *J* and *K* when clock pulse 5 occurs, so *Q* will remain HIGH.

Thank You