Triggered Devices

Digital Logic Design (CC131)

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TRIGGER

- A trigger is a control signal (usually called clock or enable) that determines when the device can change its state (output).

- Without a proper trigger, the device either holds its previous state or ignores input changes.

WHY TRIGGER IS NEEDED?

- Prevents unwanted state changes due to noise or asynchronous inputs.
- Synchronizes multiple devices in a large digital system (e.g., processors, counters, registers).
- Allows controlled data storage and transfer.

TRIGGER DEVICES

- Triggered devices are fundamental building blocks of sequential logic circuits.
- Unlike combinational circuits (where output depends only on current inputs), sequential circuits have outputs that depend on both current inputs and previous states.
- This "memory" capability comes from triggered devices.

Types of Triggered Devices

Triggered devices are mainly divided into two categories based on how they respond to the trigger signal:

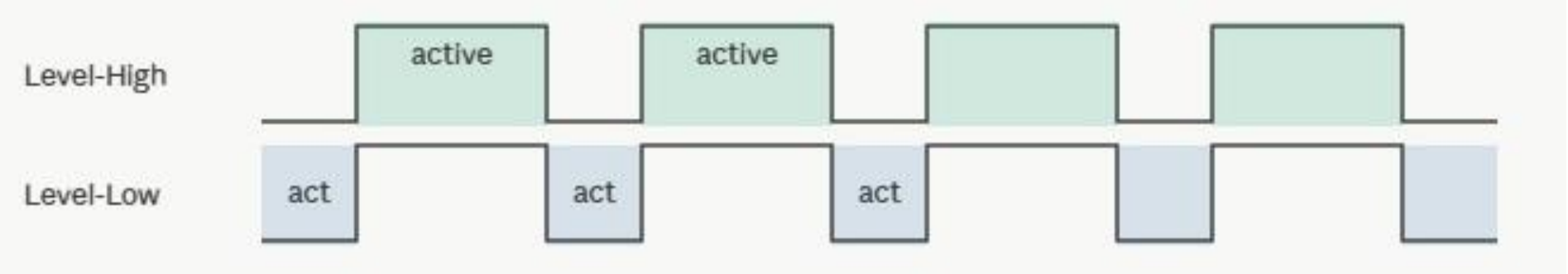
1. Level-Triggered Devices (Latches)

2. Edge-Triggered Devices (Flip-Flops)

1. Level-Triggered Devices (Latches)

In **level-triggered** devices, the output **follows the input** as long as the enable/trigger signal is active (at a certain logic level).

- **Active High (Positive Level)**: Output follows input when Enable = 1
- **Active Low (Negative Level)**: Output follows input when Enable = 0

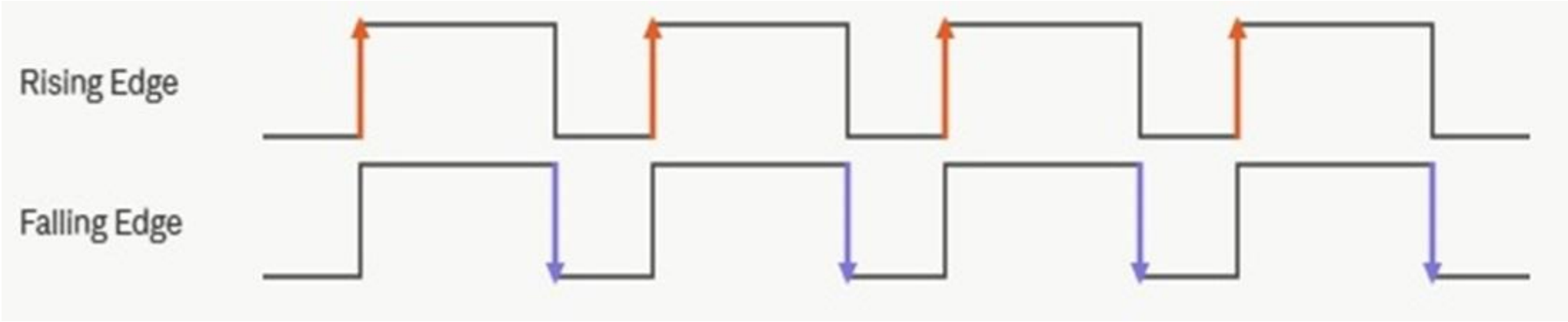


2. Edge-Triggered Devices (Flip-Flops)

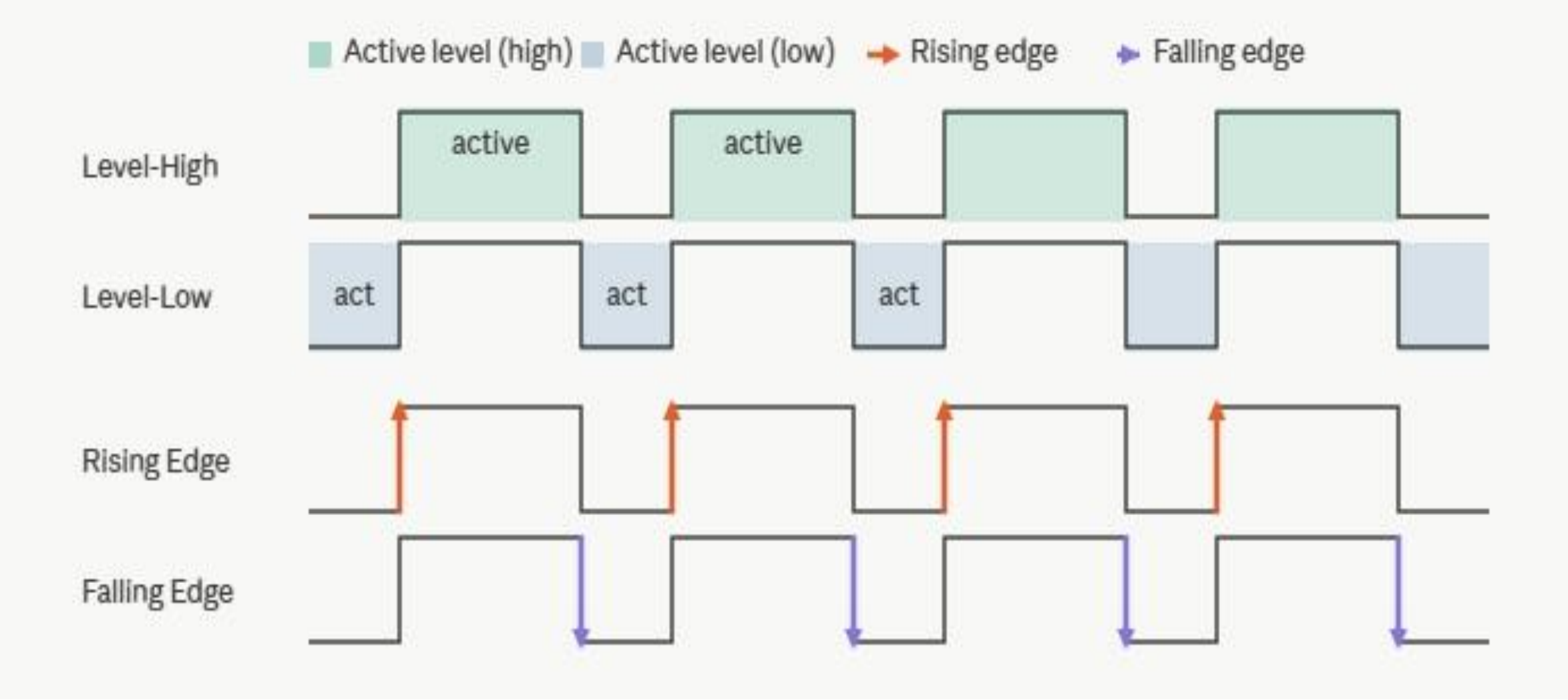
Edge-Triggered devices change their output **only at the transition** (edge) of the clock signal, not during the entire level.

Types of Edge Triggering:

- **Positive Edge Triggered** (Rising Edge ↑): Changes state at 0 → 1 transition.
- **Negative Edge Triggered** (Falling Edge ↓): Changes state at 1 → 0 transition.



Types of Triggered Devices



TYPES of Level-Triggered Devices

1. S-R Latch
2. Gated S-R Latch
3. D Latch

TYPES of Edge-Triggered Devices

1. S-R flip-flop
2. D flip-flop
3. J-K flip-flop

Comparison: Latch vs Flip-Flop

Feature	Latch (Level Triggered)	Flip-Flop (Edge Triggered)
Triggering	Level (High/Low)	Edge (Rising/Falling)
Speed	Faster	Slightly slower
Race condition risk	High	Low
Primary use	Temporary storage, glue logic	Registers, counters, FSMs
Susceptibility to noise	More susceptible	Less susceptible
Use in Synchronous Design	Limited	Preferred
Power Consumption	Generally lower	Slightly higher
Example devices	74LS373, 74HC75	74HC74 (D-FF), 74HC112 (JK)

Timing Diagrams

Key Timing Parameters:

- **Setup Time (t_setup)**: Data must be stable before clock edge.
- **Hold Time (t_hold)**: Data must remain stable after clock edge.
- **Propagation Delay (t_pd)**: Time from clock edge to output change.
- **Clock Skew**: Difference in clock arrival time at different flip-flops.

Real-World Examples

1. **Registers**: Collection of D Flip-Flops (used to store 8-bit, 32-bit data).

2. **Counters**: Made using JK Flip-Flops (Binary, Decade, Up/Down counters).

3. **Shift Registers**: Serial-in Serial-out (SISO), Parallel-in Parallel-out (PIPO) using D Flip-Flops.

4. **State Machines**: Finite State Machines (FSM) — Mealy and Moore machines use flip-flops to store states.

5. **Memory Elements**: SRAM cells use latches.

Thank You