Up / Down Synchronous Counters

Digital Logic Design (CC131)

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UP/DOWN COUNTER

- An **up/down counter** is a digital circuit that can
  count upwards (0 → 1 → 2 → 3...) **or**
  downwards (7 → 6 → 5 → 4...)
  depending on a control signal.

- **UP mode**: Counts forward.
- **DOWN mode**: Counts backward.
- One pin (called **UP/DOWN**) decides the direction:
  - **HIGH** = Up counting
  - **LOW** = Down counting

Example : 3-Bit Binary Up/Down Counter

A 3-bit counter has 3 flip-flops: **Q_2 Q_1 Q_0** (Q_0 is the Least Significant Bit).

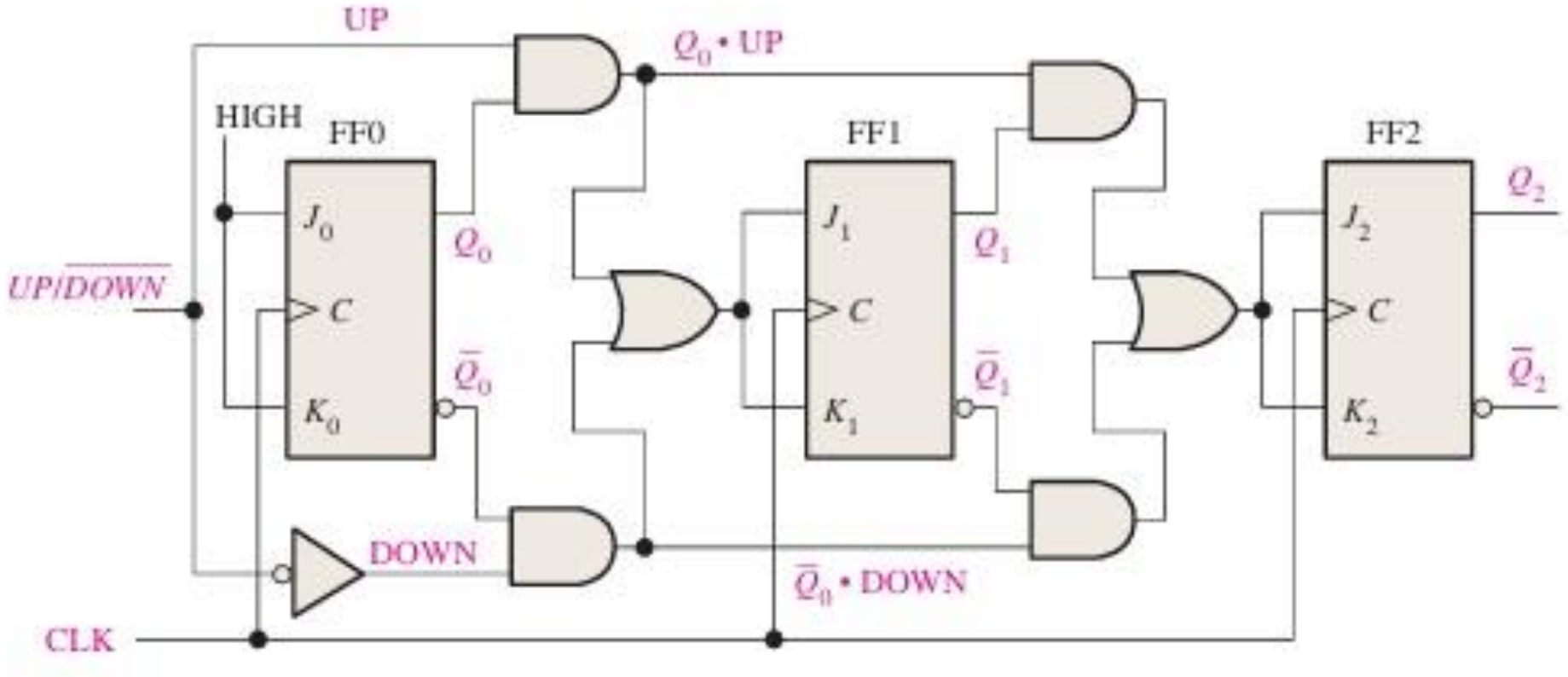
UP Sequence:

0 (000) → 1 (001) → 2 (010) → 3 (011) → 4 (100) → 5 (101) → 6 (110) → 7 (111) → 0...

DOWN Sequence:

0 (000) ← 1 (001) ← 2 (010) ← 3 (011) ← 4 (100) ← 5 (101) ← 6 (110) ← 7 (111)

Example : 3-Bit Binary Up/Down Counter



How Do We Make It Count? (The Logic)

The core idea: J-K Flip-Flops

- Each bit of the counter is stored in a J-K flip-flop (FF0, FF1, FF2).
- A flip-flop *toggles* (changes state) when its J and K inputs are both 1.
- So the trick is: *make J=K=1 only at the right moment*.

Example : 3-Bit Binary Up/Down Counter

1. FF0 (LSB - Q_0)

- Always toggles on every clock pulse (both in UP and DOWN mode).

  So: **$J_0 = K_0 = 1$** (always)

  This is same for both directions.

2. FF1 (Q_1) **When should Q_1 toggle?**

- **In UP mode**: Q_1 toggles when **$Q_0 = 1$**
- **In DOWN mode**: Q_1 toggles when **$Q_0 = 0$**

We combine both using the UP/DOWN control signal:

$$J_1 = K_1 = (Q_0 \cdot UP) + (\overline{Q_0} \cdot DOWN)$$

Simple meaning:

- If UP is active → use Q_0
- If DOWN is active → use $\overline{Q_0}$

3. FF2 (Q_2) - Most Significant Bit

When should Q_2 toggle?

- **In UP mode**: Both lower bits must be 1 → $Q_1 \cdot Q_0 = 1$
- **In DOWN mode**: Both lower bits must be 0 → $\overline{Q_1} \cdot \overline{Q_0} = 1$

So the equation becomes:

$$J_2 = K_2 = (Q_1 \cdot Q_0 \cdot UP) + (\overline{Q_1} \cdot \overline{Q_0} \cdot DOWN)$$

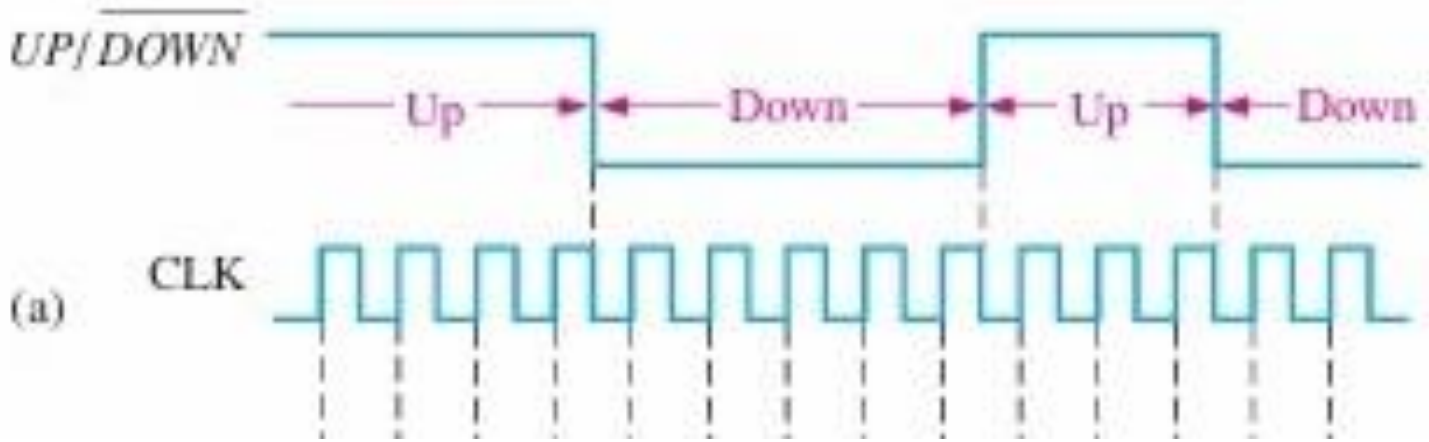
The equations are built from one simple pattern —
"a flip-flop toggles only when all the lower bits are at their boundary value".

For counting UP that boundary is all-1s.
For counting DOWN it's all-0s.

The UP/DOWN control signal just selects which condition applies, using basic AND and OR logic gates.

EXAMPLE 9–3

Show the timing diagram and determine the sequence of a 4-bit synchronous binary up/down counter if the clock and $UP/\overline{DOWN}$ control inputs have waveforms as shown in Figure 9–23(a). The counter starts in the all-0s state and is positive edge-triggered.



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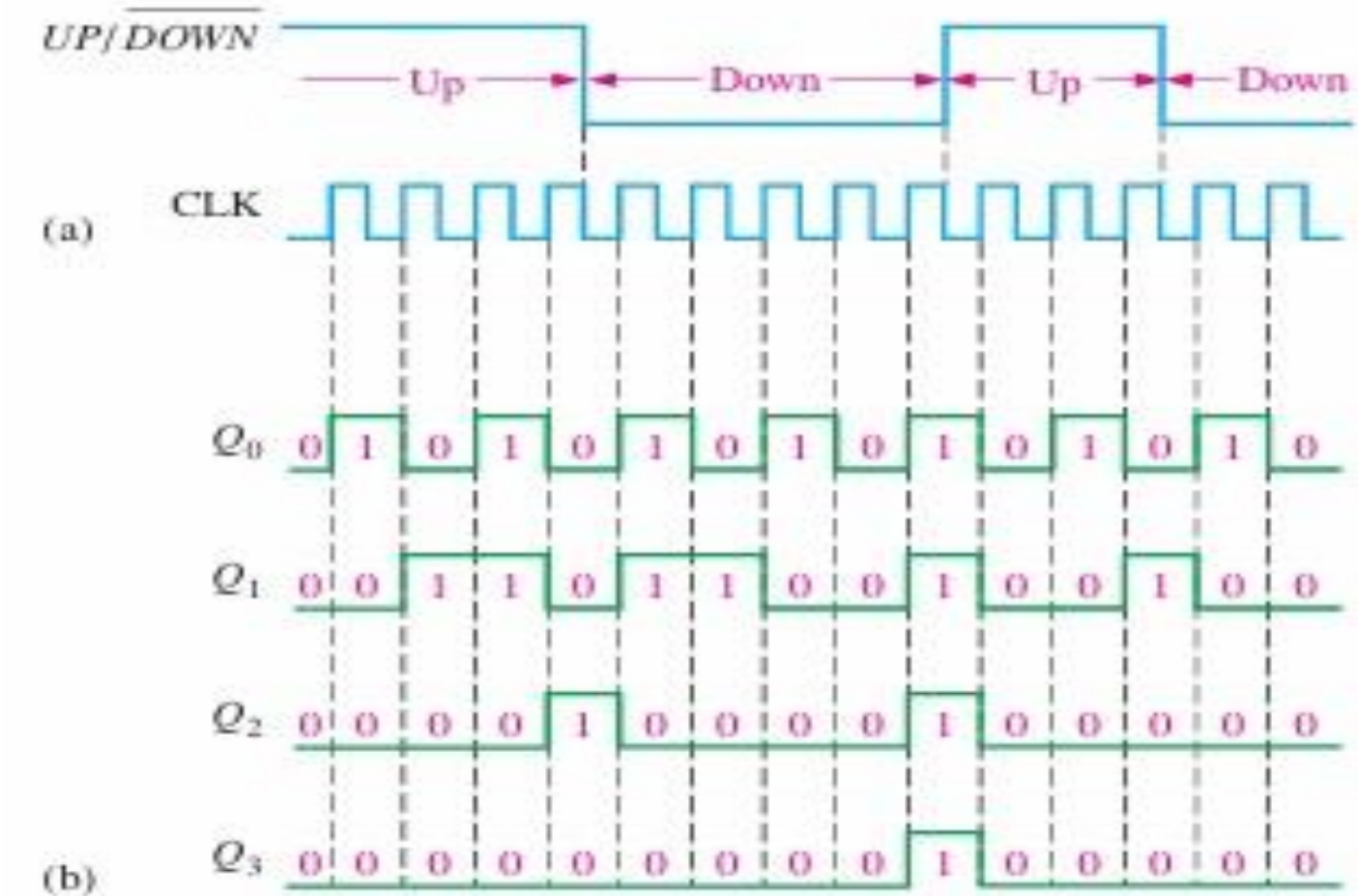

FIGURE 9–23

Thank You